A Light Speed Optical Approximate Parallel Multiplier and Its Applications

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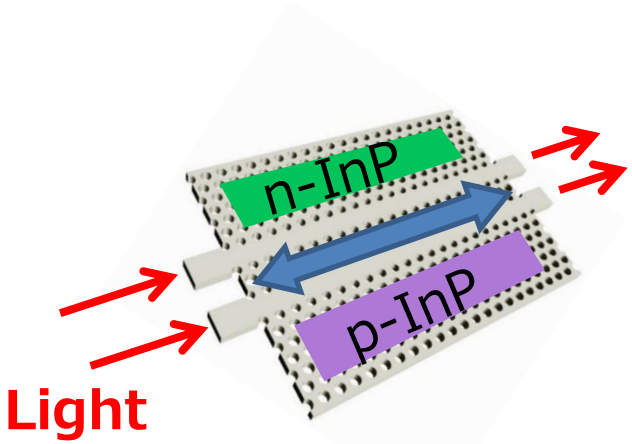
Integrated Optical Logic Circuits Using Nanophotonics



Device length ~ 100 μm

E.g. Photonic crystal-based directional coupler

✓ Direction control on the order of the light wavelength

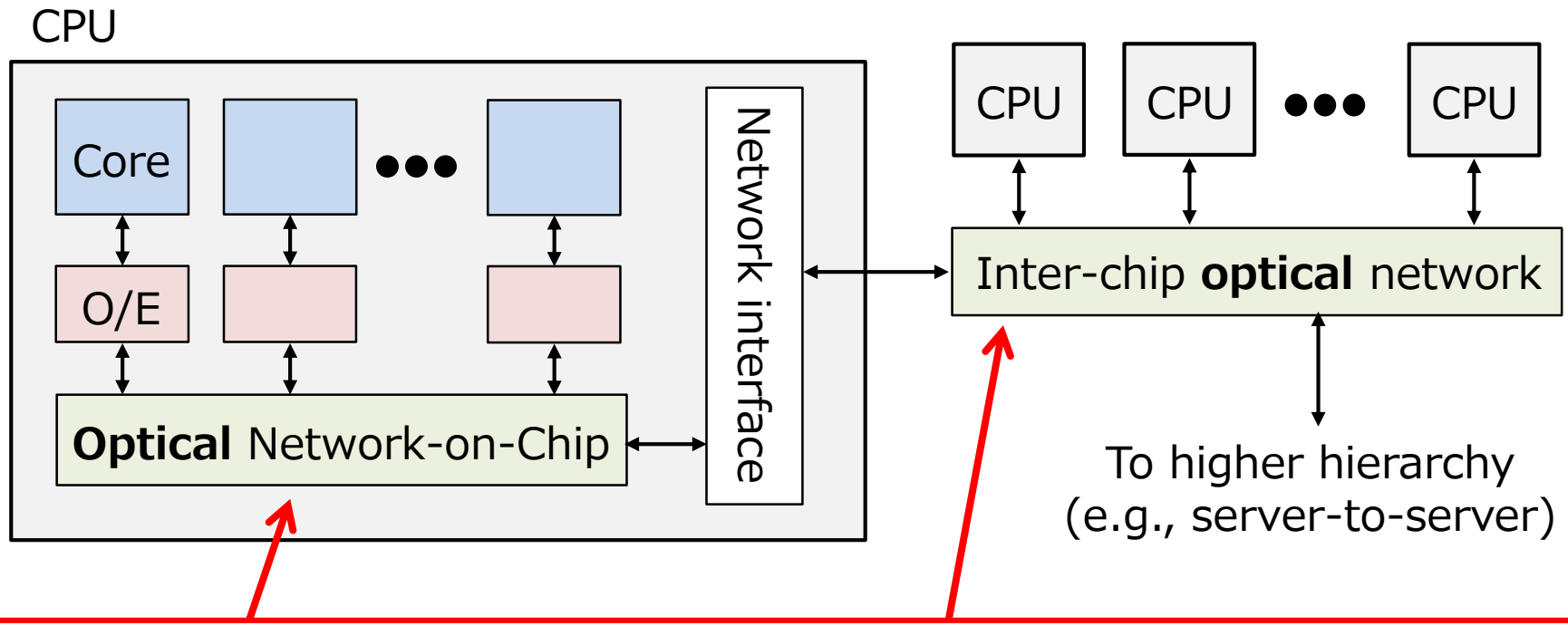
➡
- ☺ On-chip implementation
- ☺ **Ultra-low latency**

CMOS logic gate	~ 10 ps
Nanophotonics-based	0.1 ps ~ 1 ps

Goal: Ultra-fast optical logic circuit design

Beyond Optical Communication

Existing technique's focus: on-chip optical communication



Goal: Add **functional unit** to boost up on-chip communication

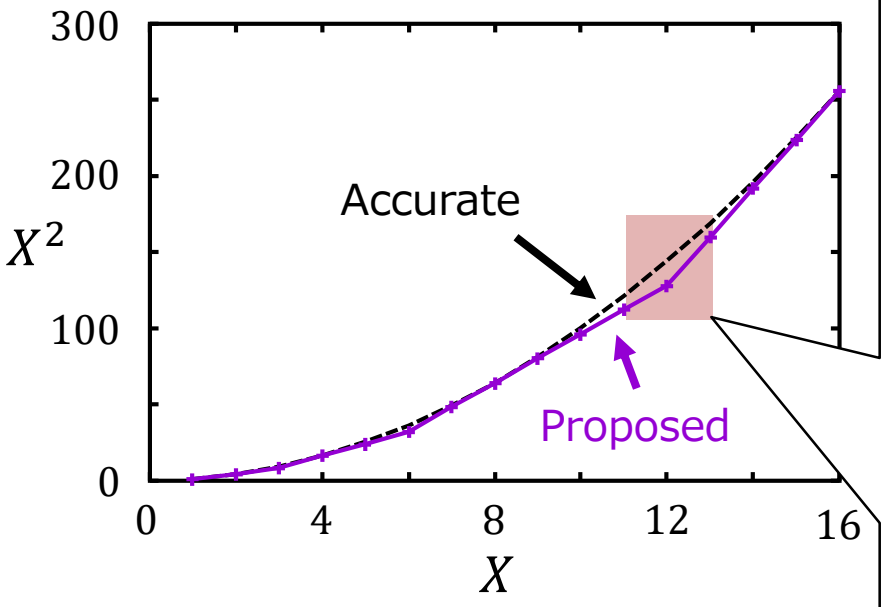
➡ E.g. Pattern recognition circuit for packet filtering

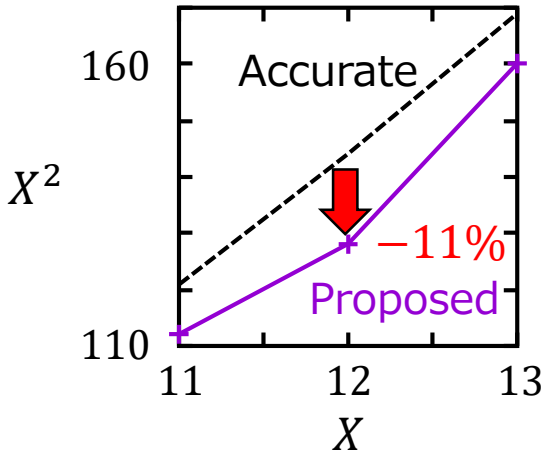
Fully-Digital Approximate Parallel Multiplier Consisting of Priority Encoder and Barrel Shifters Only

☺ Ultra-fast operation (Low latency)

- ~ 10 GHz for 16b multiplication
- About 3 × faster than electrical multiplier

☹ Deterministic multiplication error (up to −11%)

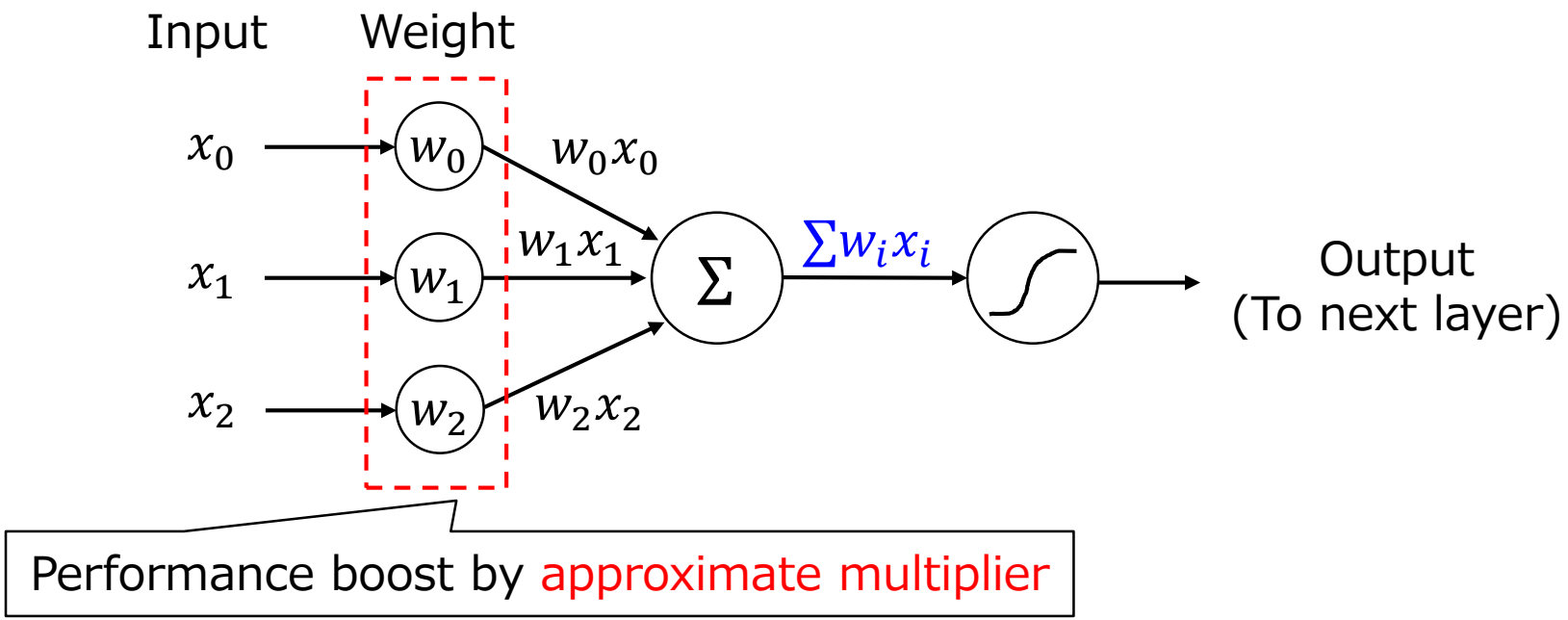




✓ Piecewise linear approximation
✓ Fixed error at every calculation

Application Example: Pattern Recognition

E.g. Neural Network



- ✓ Pattern recognition: high resiliency to approximation errors
- ✓ Absorb the deterministic error by learning process

$$\boldsymbol{w_0}x_0 + \boldsymbol{w_1}x_1 + \boldsymbol{w_2}x_2$$

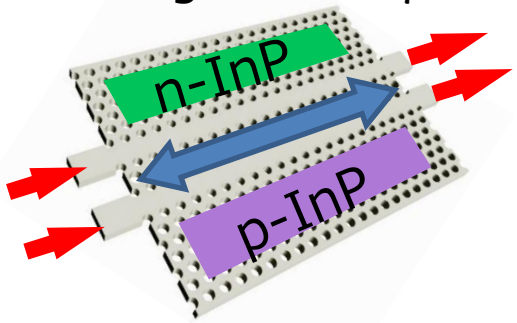
Weight vector optimization to cancel out **deterministic** error

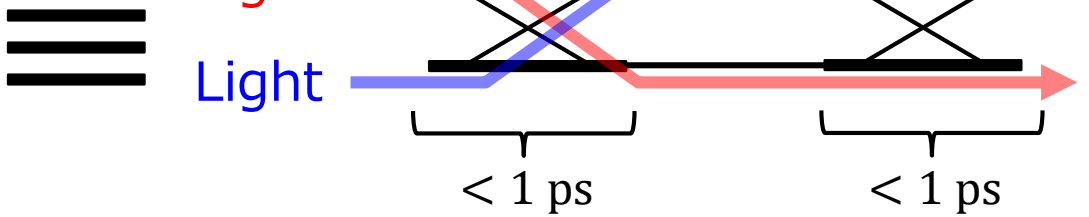
Outline

- Background
- Parallel Multiplier Using Nanophotonic Devices
- Proposed Approximate Parallel Multiplier
- Performance Evaluation
  - Speed and accuracy
  - Power
- Conclusion

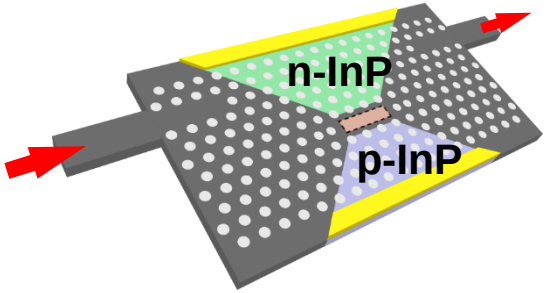
Photonic Crystal-Based Optical Pass-Gate (OPG)

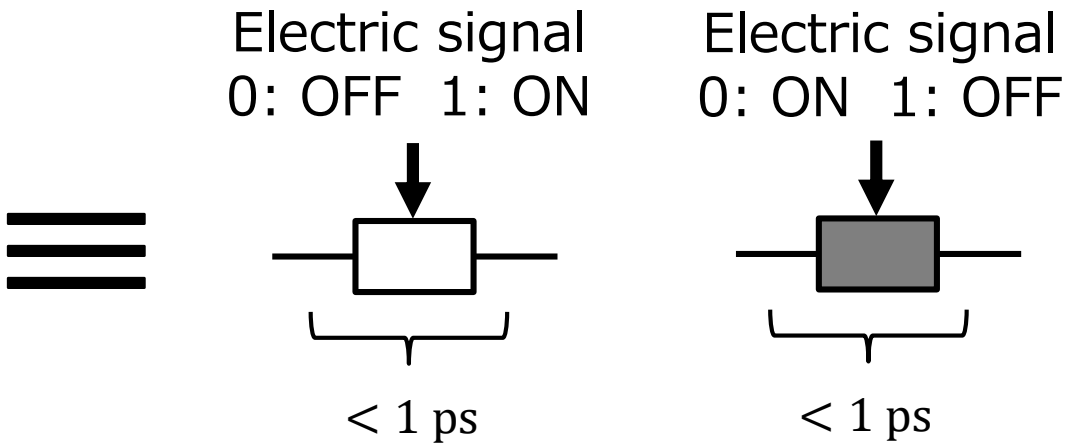
Directional coupler





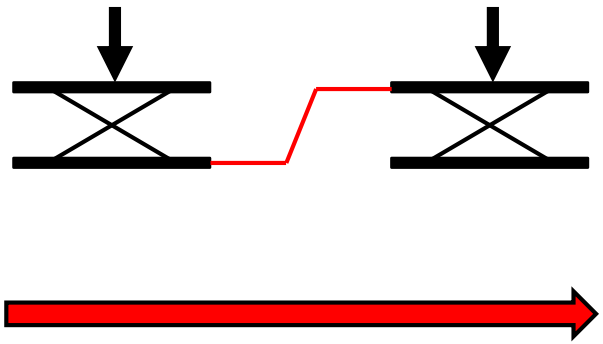
Modulator (switch)





OptoElectric (OE) Conversion Delay

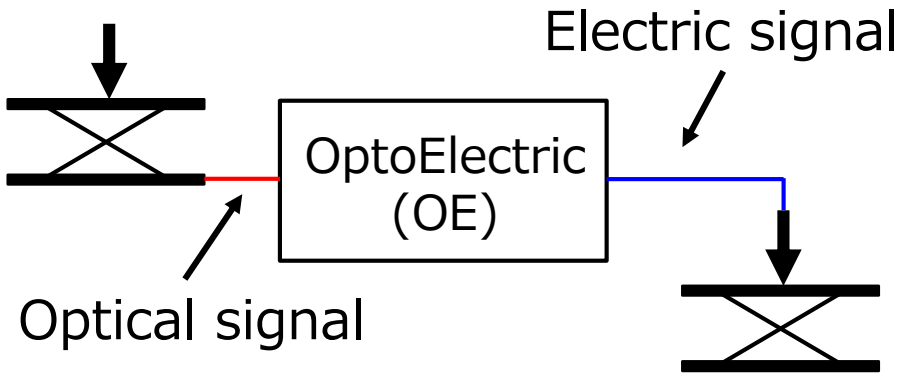
Serial connection



Light speed (~ **1 ps**/gate)

τ_{sw}

Cascade connection



OE conversion (~ **25 ps**/OE)

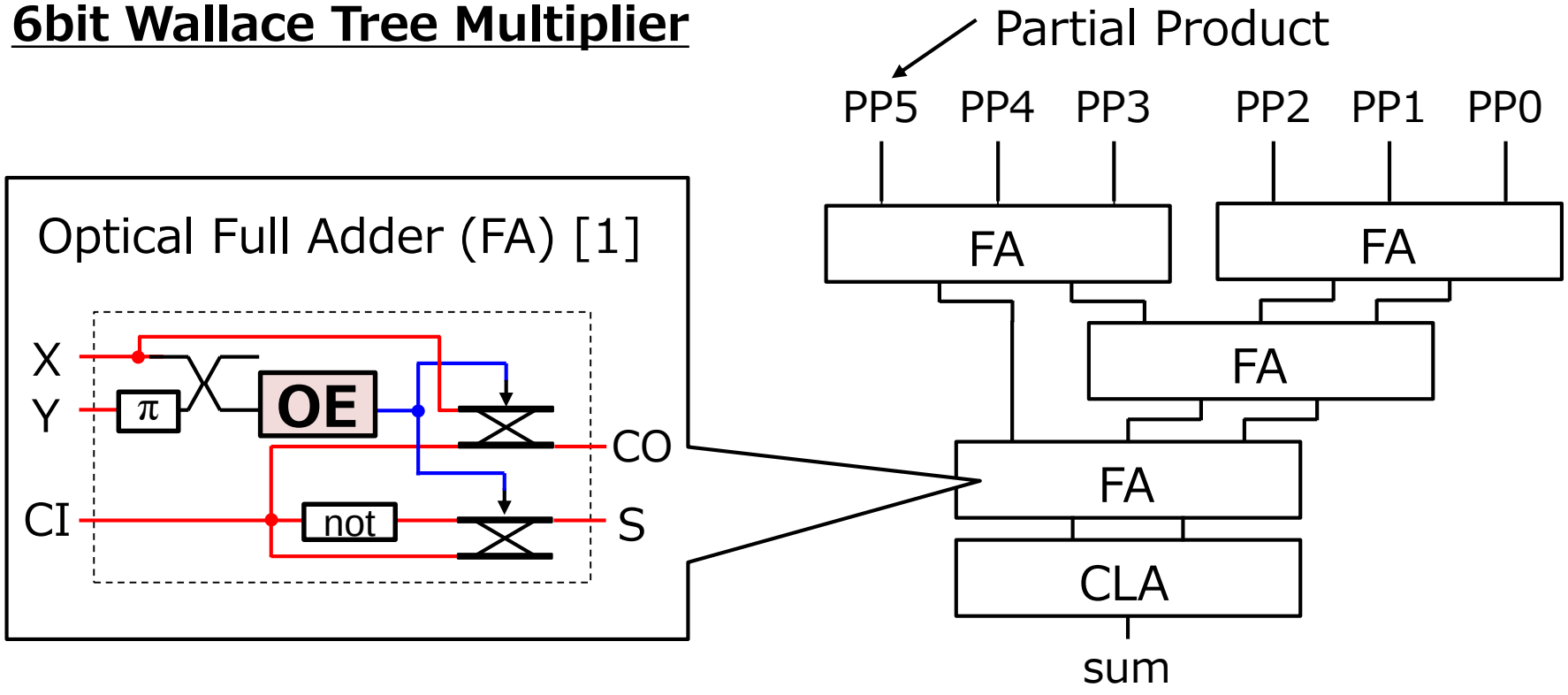
τ_{oe}

✓ **Reducing OEs on a critical path** is a key to ultra-fast operation

cf. CMOS ~ 10 ps/gate

Issues in Conventional Optical Parallel Multiplier

6bit Wallace Tree Multiplier



☹ Large #(OEs on critical path) for large bit width n

⇨ Unacceptable latency for large n

[1] T. Ishihara, et al., International SoC Design Conference, 2016

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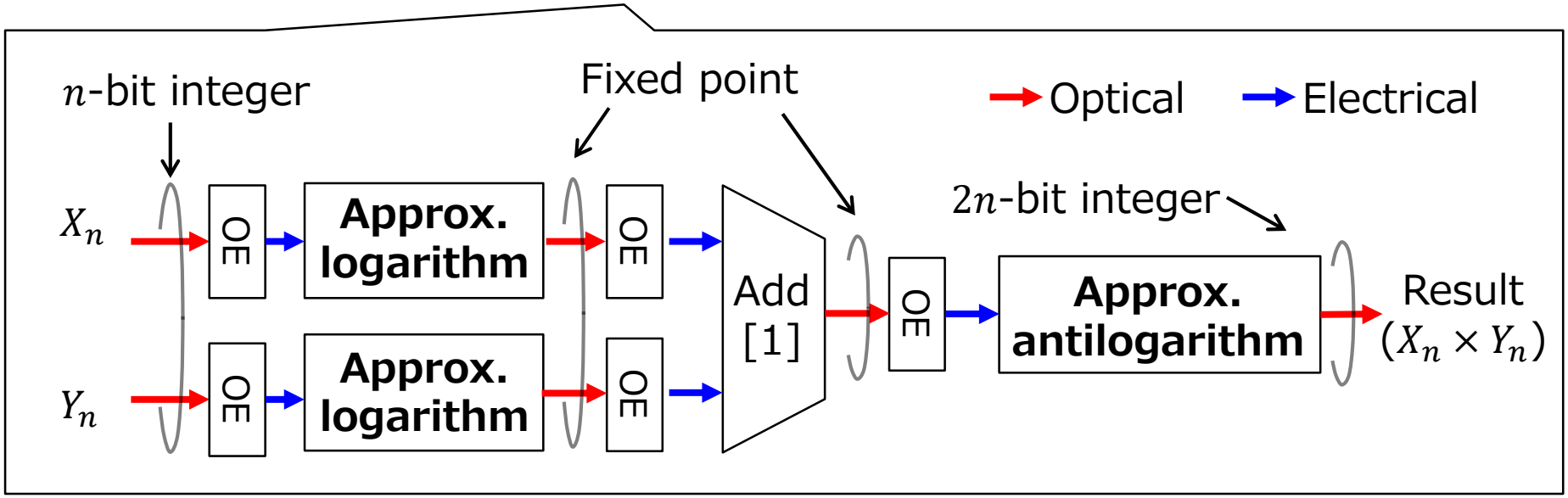
Basic Idea of the Proposed Approximate Multiplier

$$X_n \times Y_n = 2^{\log_2 X_n + \log_2 Y_n} \qquad (X_n, Y_n \in \mathbb{Z}_+)$$



✓ { Approximate log / Accurate addition / Approximate antilog } : one OE conv. + serial connection only

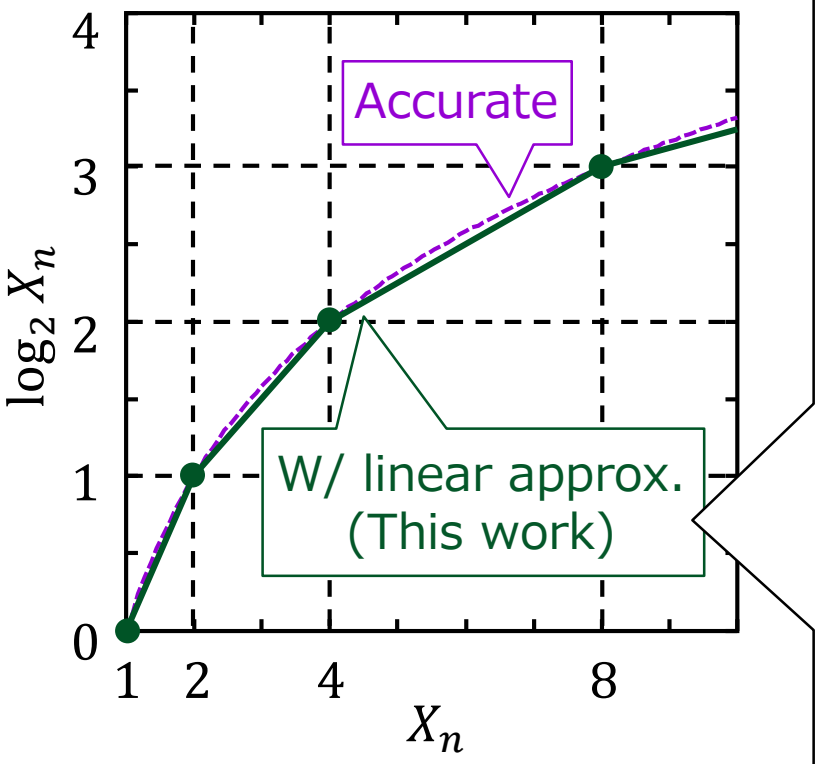
➡ Only three OE converters on critical path

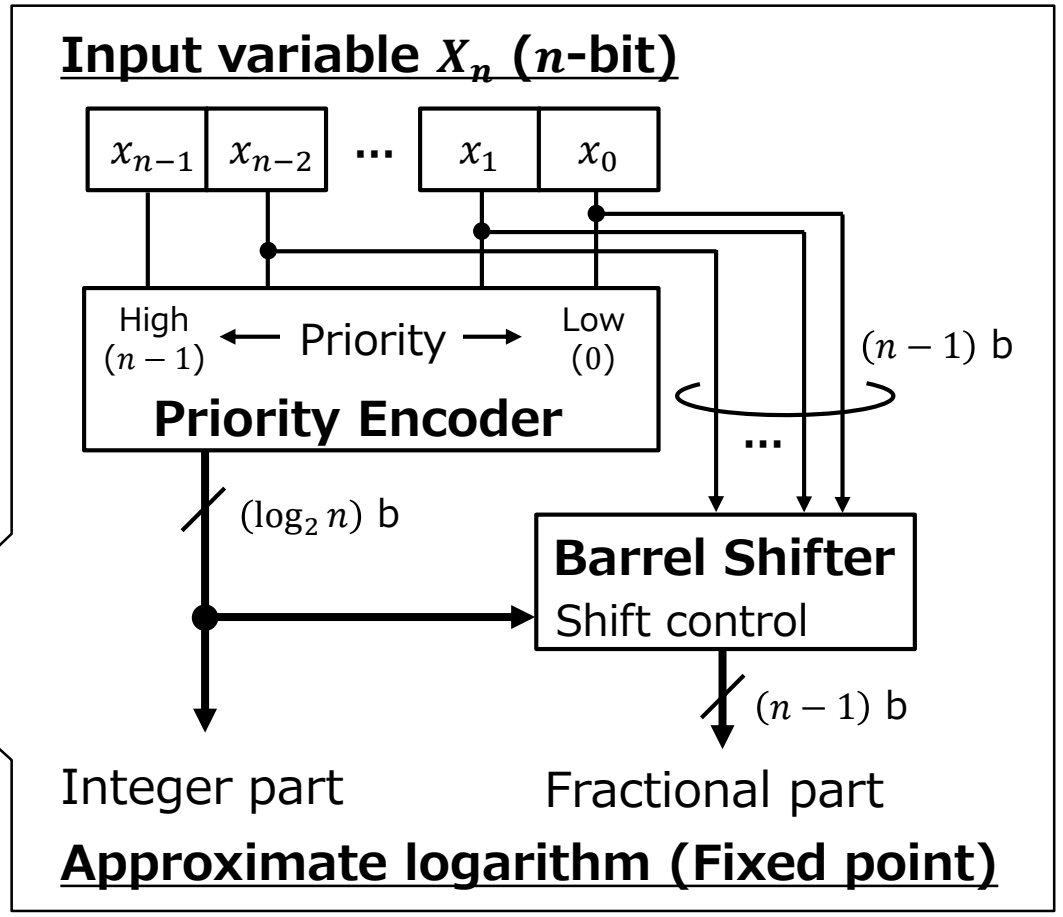
[1] T. Ishihara, et al., International SoC Design Conference, 2016

Concept of Approximate Logarithm [2]

$2^{\log_2 X_n + \log_2 Y_n}$

[2] J. N. Mitchell, IRE Transactions on Electronic Computers, 1962

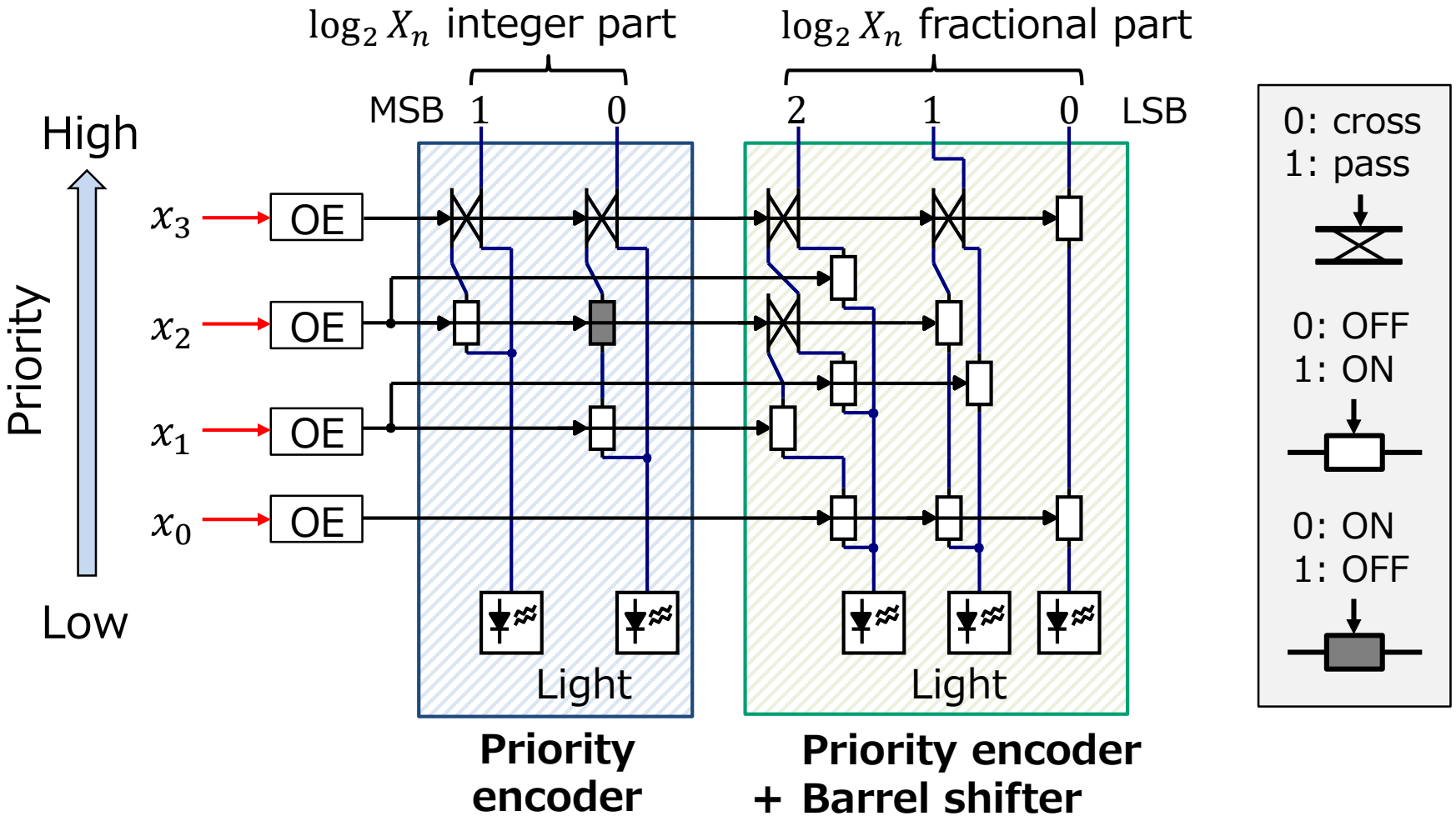




- ✓ Priority encoder & barrel shifter: typical circuit in optical network
- ✓ Antilogarithmic function ⇒ Inverse function of logarithm

Optical Implementation of Logarithm ($n = 4$)

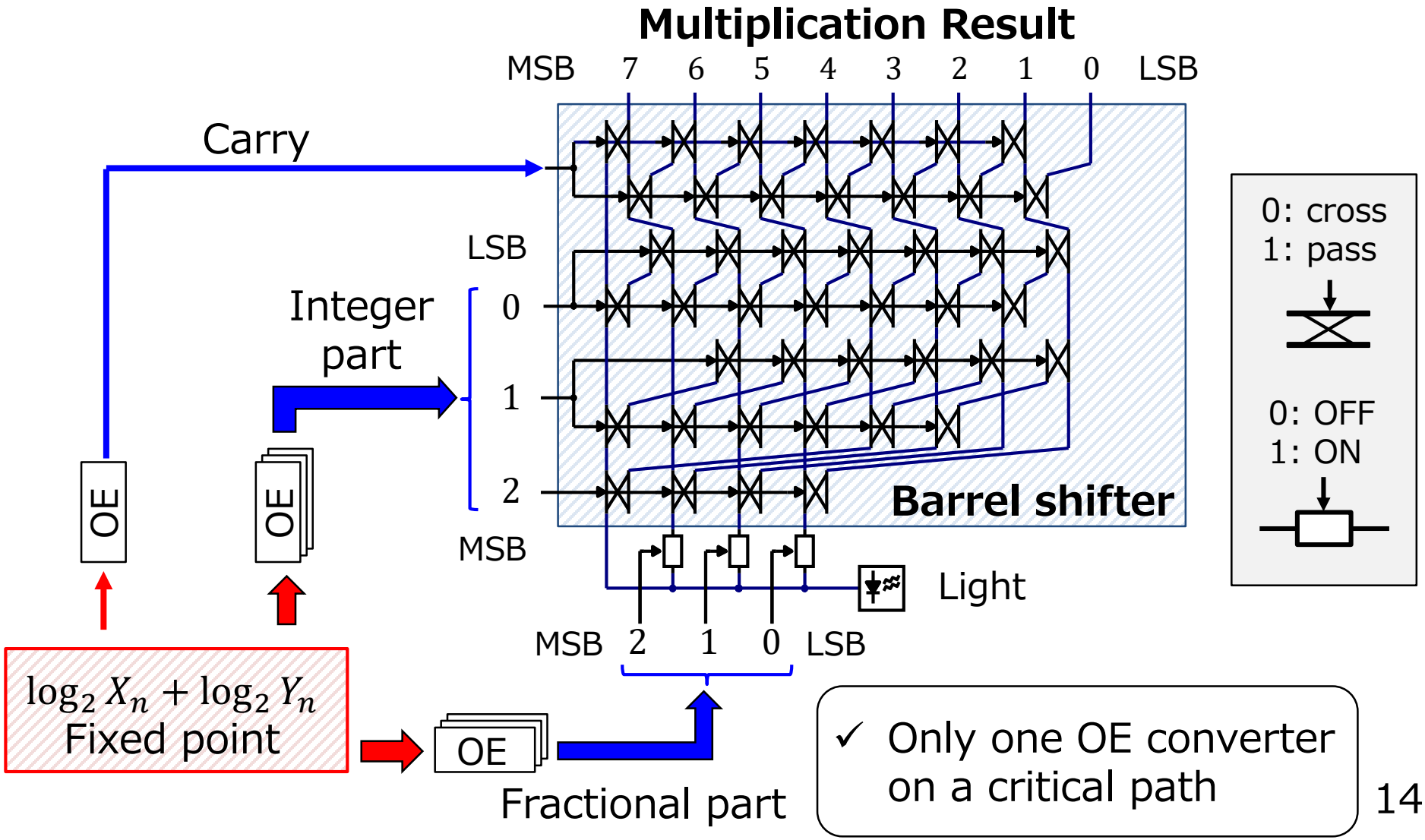
$2^{\log_2 X_n + \log_2 Y_n}$



✓ Only one OE converter on a critical path for any n

Barrel Shifter-Based Approximate Antilogarithm ($n = 4$)

$2^{\log_2 X_n + \log_2 Y_n}$



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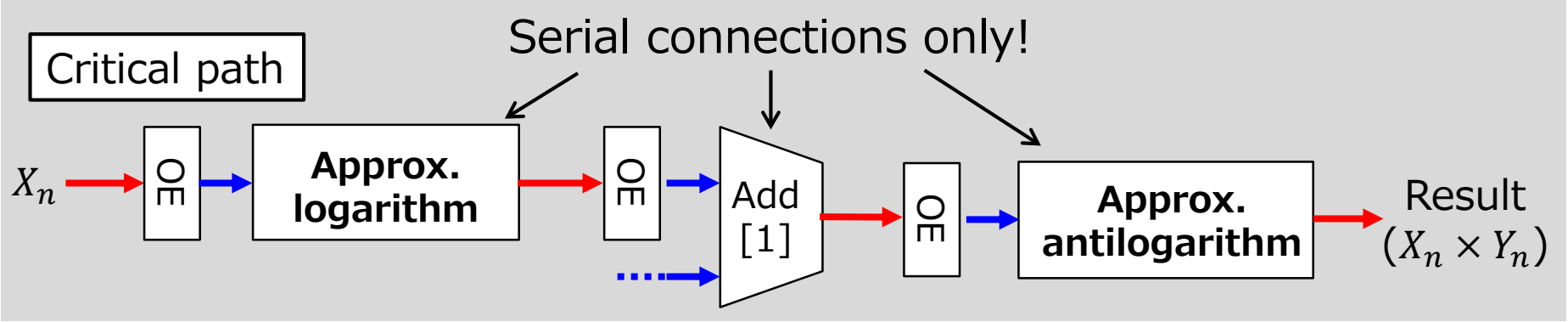
Performance Analysis (Latency, Error)



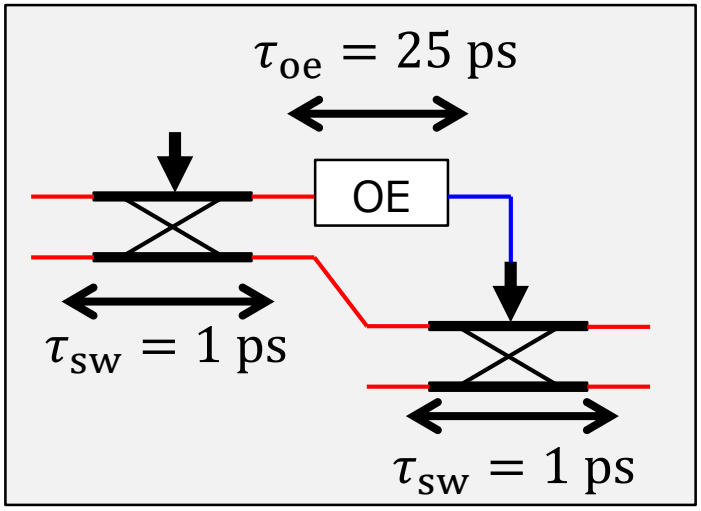
✓ Latency $= 3\tau_{\mathrm{oe}} + O(n\tau_{\mathrm{sw}})$

τ_{oe}: 25 ps, τ_{sw}: 1 ps

✓ Deterministic error [2]

-11% $(X_n = 3 \cdot 2^i$ AND $Y_n = 3 \cdot 2^j)$

0% $(X_n = 2^i$ OR $Y_n = 2^j)$ $i, j \in \mathbb{Z}_{\geq 0}$



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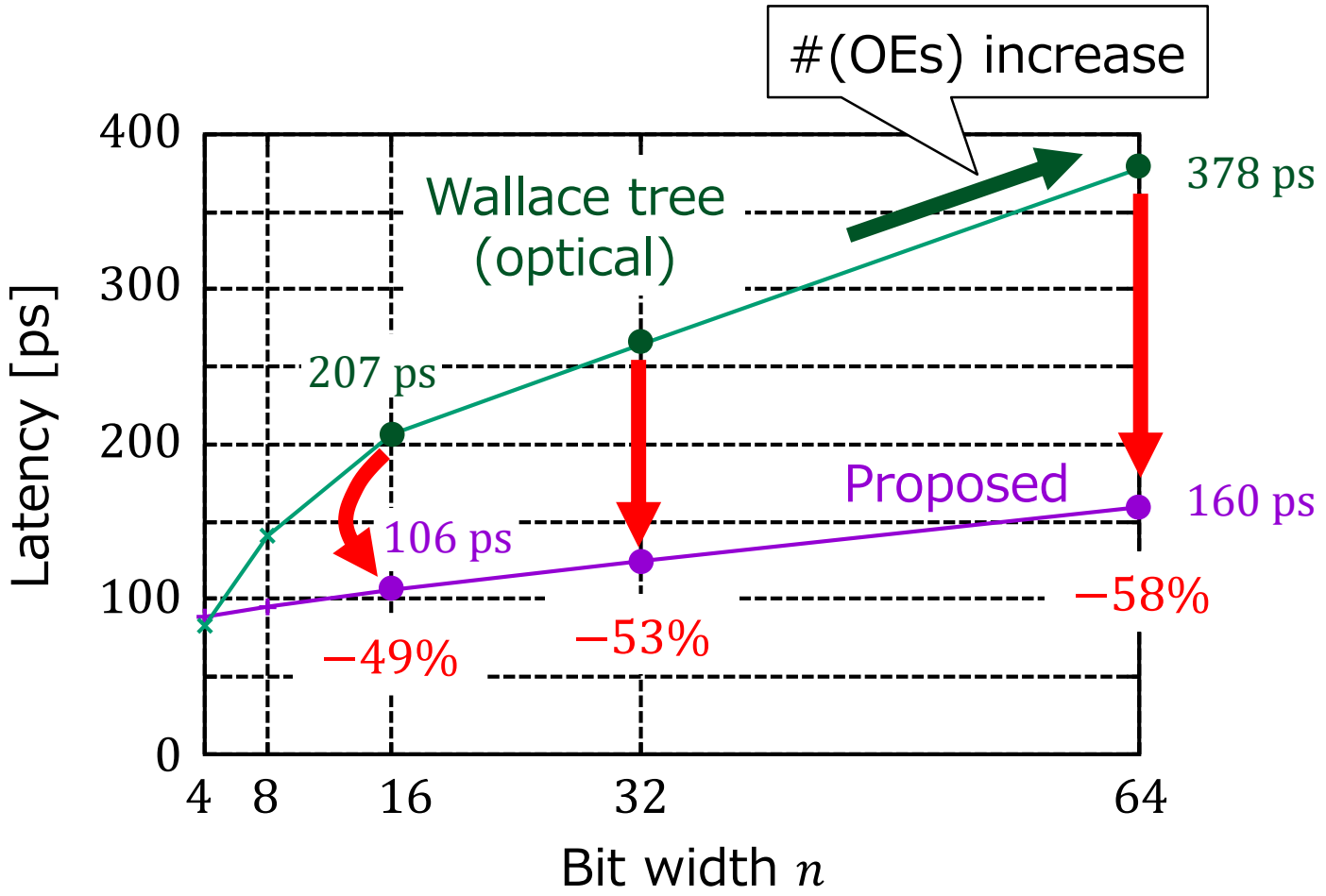
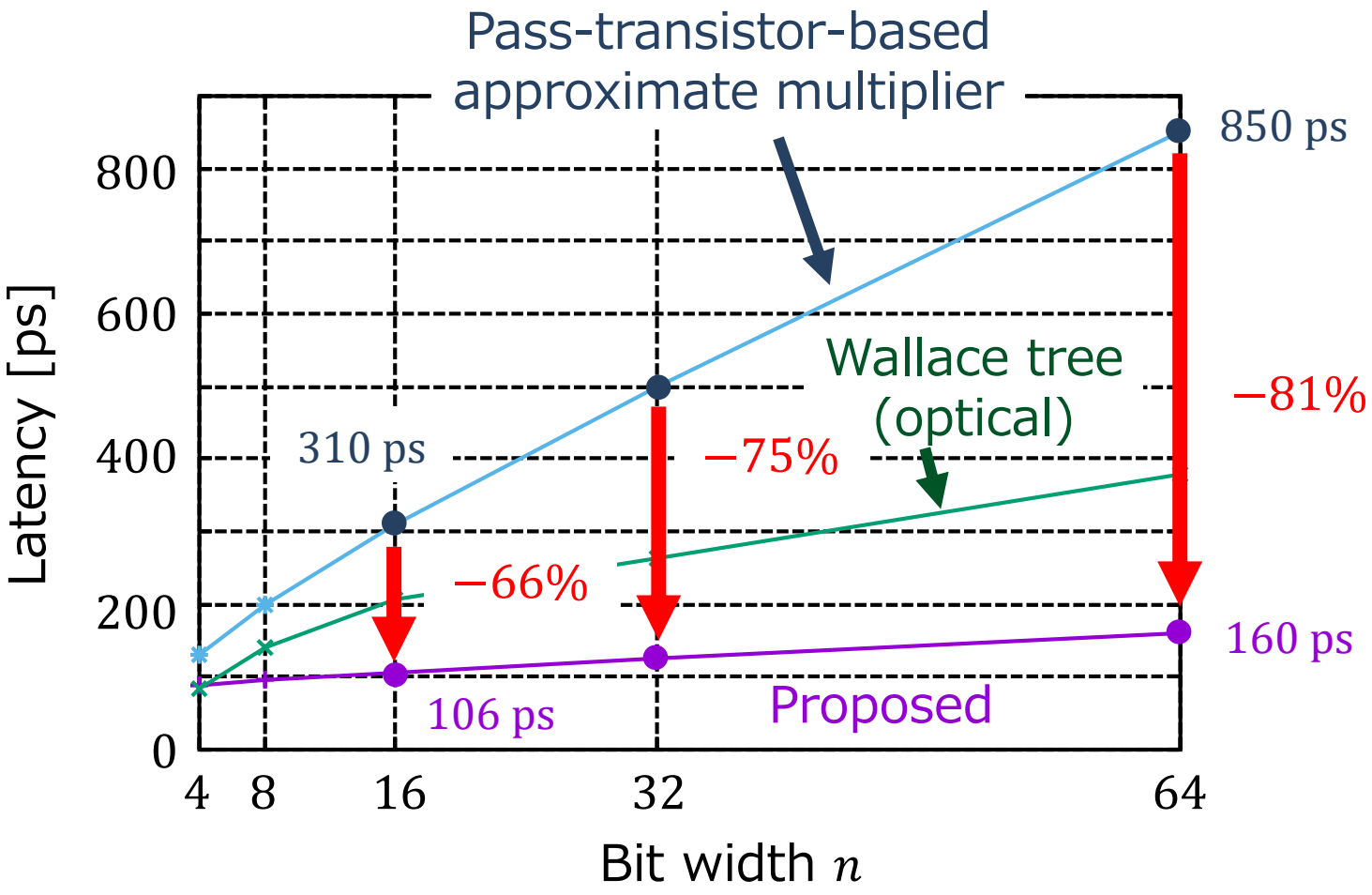
[2] J. N. Mitchell, IRE Transactions on Electronic Computers, 1962

Optical Multiplier Latency Comparison: Accurate Multiplier vs. Approximate Multiplier



✓ About 2 × faster than naive optical multiplier

Latency Comparison: Pass-transistor-based vs. Approximate Optical Multiplier



✓ More than 3 × faster than conventional multiplier

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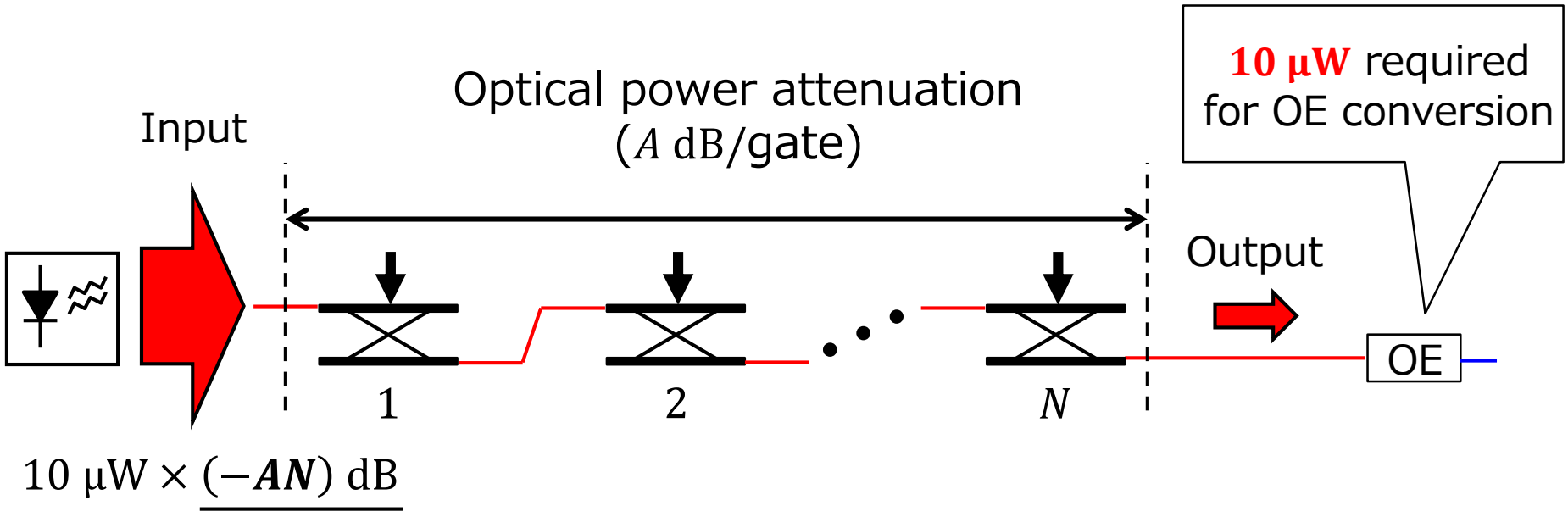
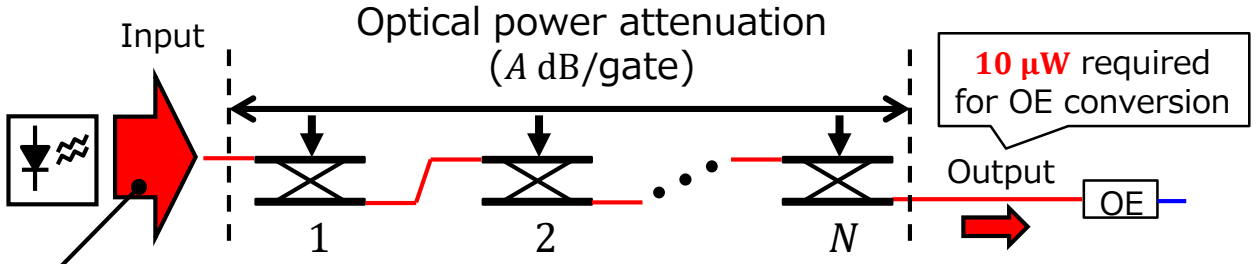
Power Dissipation Mechanism in Optical Circuitry

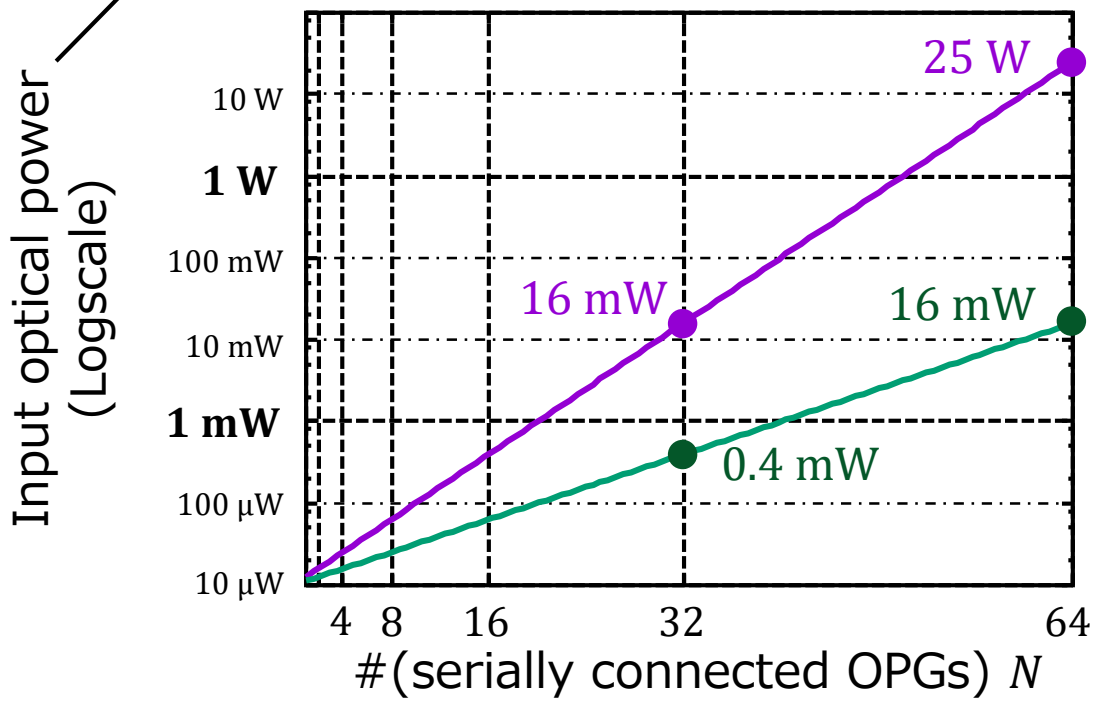


☹ Light source power: exponentially proportional to N

✓ May limit the scalability of the proposed multiplier

Power Dissipation of Serially Connected Circuit





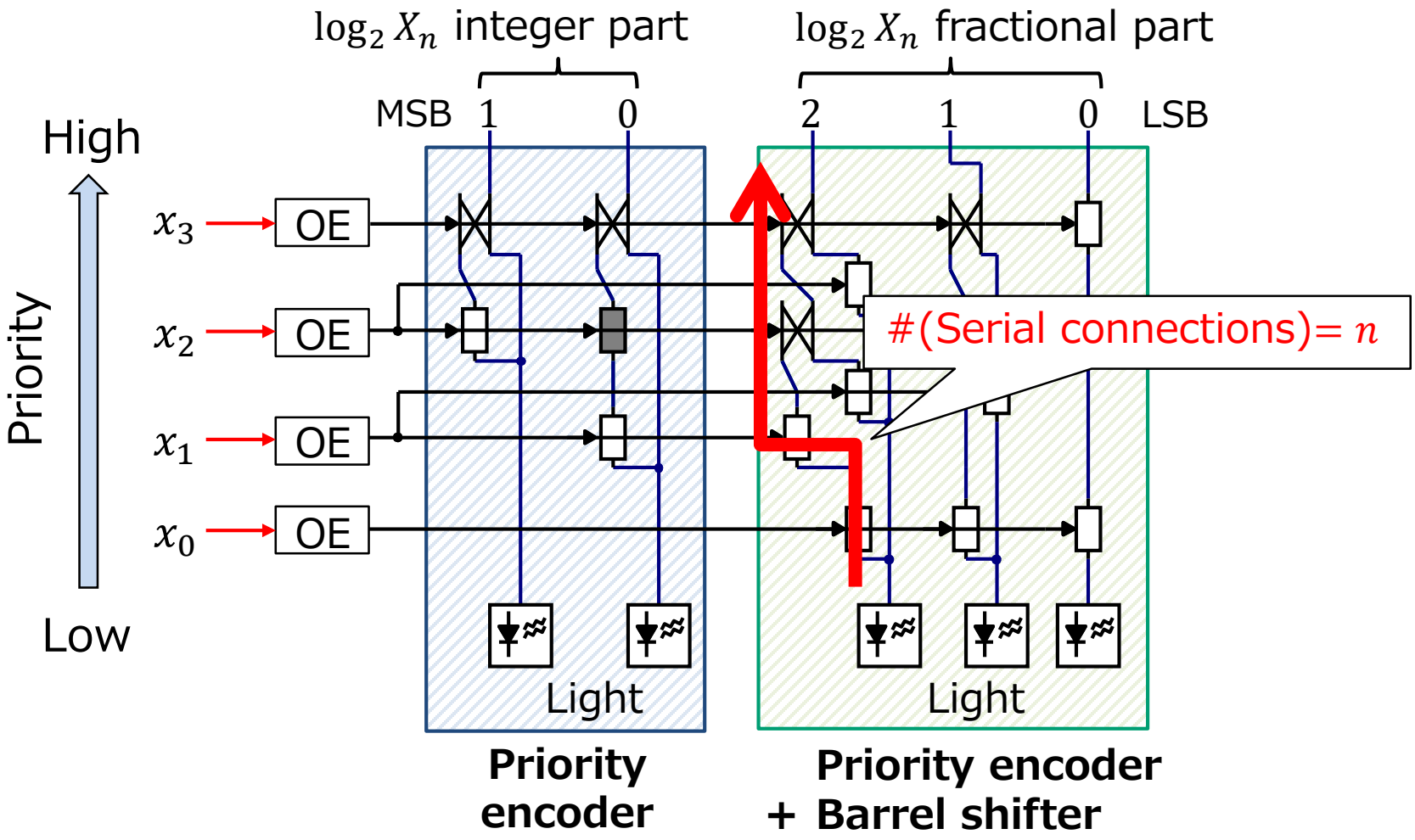
$A = -1$ dB/gate
(Typical OPG performance)

Device improvement

$A = -0.5$ dB/gate

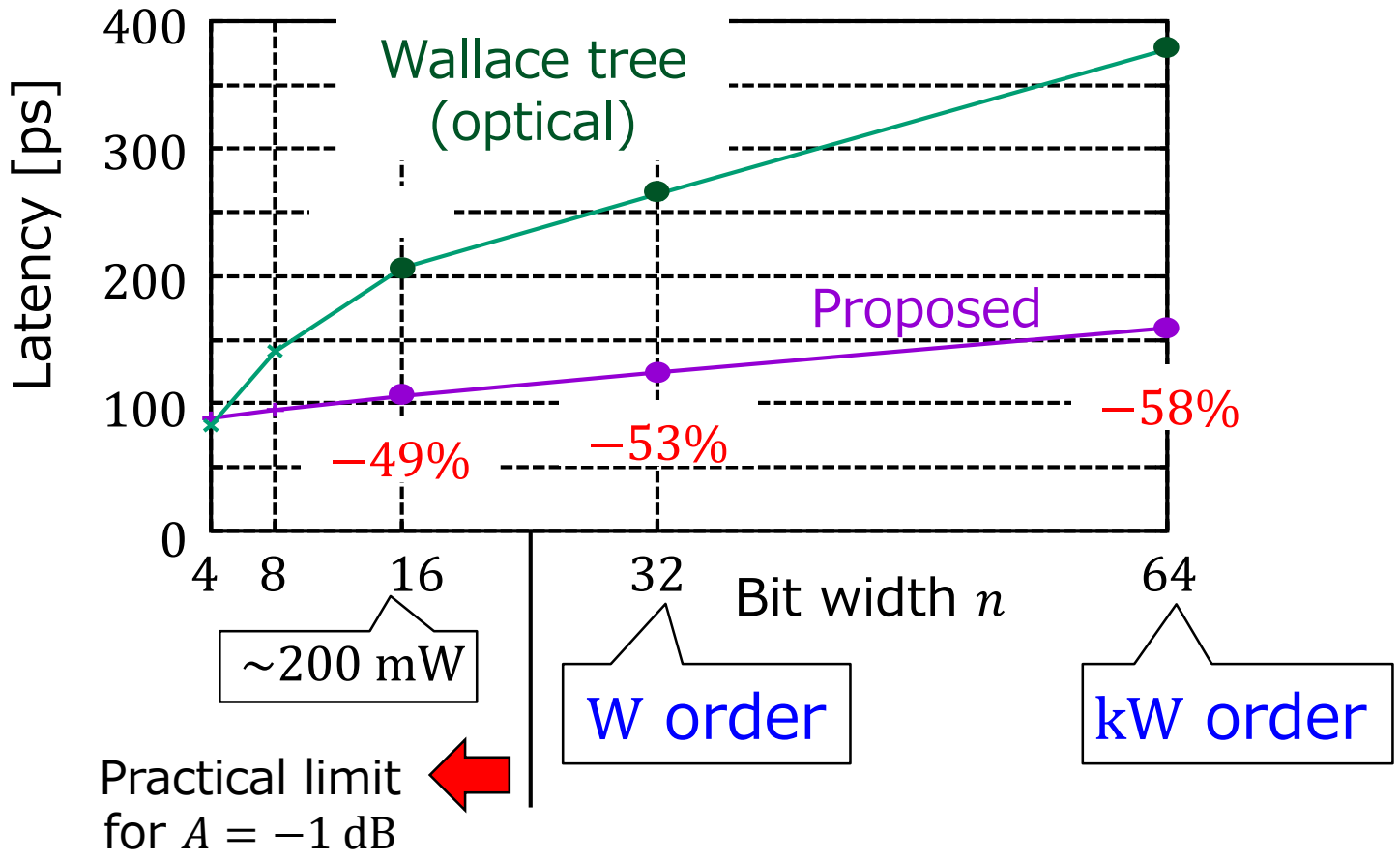
✓ Material (A) improvement is a key for ultra-fast multiplication

Optical Implementation of Logarithm ($n = 4$)



✓ Exponential power explosion for large n

Power Dissipation Estimation Results ($A = -1\,\mathrm{dB}$)



✓ Material (A) improvement is a key for ultra-fast multiplication

Conclusion and Future Work

✓ Optical Approximate Parallel Multiplier for Pattern Recognition

- Low latency: 106 ps for 16-bit multiplication

  → About 2 × faster than naïve optical multiplier
  → About 3 × faster than electrical multiplier

- Deterministic error: from −11% to 0%

• Future Work

- Power dissipation reduction technique
  - Architectural-level optimization
  - Material (Attenuation) improvement is also a key
- Implementation of the multiplier into practical pattern recognition frameworks