Enhanced Silicon Photonics Platform for High Performance Many-Core Processors

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21/10/2018 – PHOTONICS2018
IRT / LETI Context
High level goals

21/10/2018
IRT at a glance

• IRT (French Institute of Technology) are public financed programs targeting technological developments to serve the French industry.

• IRT Nanoelec:
  – Targetting µ-electronics technologies
  – Silicon Photonics, 3D EIC assembly, GaN power devices, Material Characterisation
  – 19 Partners, 50M€ annual budget
PHOTONICS AT LETI

French research-and-technology organization with activities in energy, IT, healthcare, defence and security. Budget 318 M€.

1,900 collaborators (250 PhDs)
2800 patents (>300 /yr)
680 publications /yr, 64 startups

8,500 m² clean rooms
For 200 and 300 mm wafers fab, operated 24/7

Photonic Department
Est. 1978, 300 researchers, 60M€ budget
Dedicated Silicon Photonics Lab
200mm Si Photonics platform
310nm Si height

21/10/2018
Technological Platform Ecosystem

300mm STm Si Pho. Industrial Platform

Core process 200mm
(Si etch: strip, shallow rib, deep rib/Pn junction/Resistive Heaters)

Ge epi
2 levels BEOL
Frontside cavity

SiN

3D Add-on
(Cavities, TSV, UBM, microbumps)

• WDM
• Edge coupler
• Low loss waveguide

III-V Add-On

• Photonic interposer
• ONoC

• Laser integration
• EAM, SOA

Industrial Platform

SiN

WDM
Edge coupler
Low loss waveguide

Laser integration
EAM, SOA
200mm Core Technological Platform

• 200 mm Si photonics platform
  - Substrates: 8” SOI 310nm, compatible with ST foundry
  - 190 steps
  - 24 litho levels
  - 40 metro/control steps

• Process building blocks
  - Multilevel silicon patterning
  - SiN guiding layer
  - PN Silicon junctions
  - PiN Germanium junctions
  - Integrated resistance (heater)
  - Planarized BEOL: 2 AlCu routing levels
  - UBM for flip-chip assembly
200mm Core Technological Platform

- Passive Device Library @ 1310nm

<table>
<thead>
<tr>
<th>Width</th>
<th>Prop. loss</th>
<th>Ins. Loss</th>
<th>1dB BW</th>
<th>Xtalk</th>
<th>Loss</th>
<th>balance</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 nm</td>
<td>1.5 dB/cm</td>
<td>&lt; 3 dB</td>
<td>30 nm</td>
<td></td>
<td>&lt; 0.5 dB</td>
<td>±3%</td>
</tr>
<tr>
<td>1.8 µm</td>
<td>0.15 dB/cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>320 nm</td>
<td>3.5 dB/cm</td>
<td>&lt; 5 dB</td>
<td>30 nm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>350 nm</td>
<td>3.5 dB/cm</td>
<td>2-3 dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

... Equivalent Device Library @ 1550nm
200mm Core Technological Platform

• High Speed MZM for O-band and C-band

<table>
<thead>
<tr>
<th>MZM Length</th>
<th>Vpi.Lpi</th>
<th>RF BW 3dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>4mm</td>
<td>1.9 V.cm</td>
<td>25GHz</td>
</tr>
<tr>
<td>3mm</td>
<td>1.9 V.cm</td>
<td>28GHz</td>
</tr>
<tr>
<td>2mm</td>
<td>1.9 V.cm</td>
<td>35GHz</td>
</tr>
<tr>
<td>Losses</td>
<td>0.55 dB/mm</td>
<td></td>
</tr>
</tbody>
</table>
200mm Core Technological Platform

• High Speed Silicon Ring Modulator for O-band

R = 6µm
FSR = 10.5nm
Counter Doped
Mod. Eff. = 1.55 V.cm at -1V

5Gbps
10Gbps
1.2Vpp drive voltage
200mm Core Technological Platform

- High Speed SiGeSi photodetector

<table>
<thead>
<tr>
<th>Width</th>
<th>0.8µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>15µm</td>
</tr>
<tr>
<td>Responsivity</td>
<td>&gt; 1.05A/W</td>
</tr>
<tr>
<td>Dark current @ -2V</td>
<td>5 nA</td>
</tr>
<tr>
<td>BW @ -2V</td>
<td>&gt; 40GHz</td>
</tr>
</tbody>
</table>

B. Szelag et al., SSDM 2017
200mm Technological Platform SiN Add-on

- SiN layer
  - Adiabatic/Edge couplers
  - Propagation losses: 0.8 dB/cm (w=700 nm w x h=600 nm)
  - Si/SiN transitions: < 0.1 dB (Si h=150 nm, length 150 µm)
  - athermal Mux/DEMUX

- Performance
  - Insertion loss: -1.5 dB (avg.)
  - Xtalk (min): -30 dB (avg.)
  - Non uniformity: 1.5 dB
  - -1dB BW: 8 to 10 nm
  - -1dB Xtalk: -15 dB to -22 dB
  - Thermal shift: 13 pm/°C

C. Sciancalepore et al., Proc of SPIE Phot. West 2018
Q. Wilmart et al., in Proc. of SPIE Phot. West 2018
200mm Technological Platform SiN Add-on

- SiN assisted Si surface grating coupler
  - Gratings both in Si and SiN
  - Grating relative shift controls directionality
  - Enhanced bandwidth

Experimental results
- Minimum I.L. : 2.8 dB
- -1dB BW : 48 nm
- I.L. over CWDM band: min / max = 3 / 5.8 dB
  (compared to 1.9 / 13 dB for Si apodized design)

Q. Wilmart el al., in Proc. of SPIE Phot. West 2018
200mm Technological Platform 3D Add-on

- THROUGH SILICON VIAS / PHOTONIC INTERPOSER

TSV last on SOI wafer

“System-in-package”

Abs(S12)

Ribbon bonding

TSV Ø 80

TSV Ø 60

S. Bernabé, K. Rida, S. Menezo,

L. Fourneaud, Internal report
200mm Technological Platform III-V (Laser) Add-on

- III-V die bonding / patterning for integrated laser sources in silicon

- Growth of the III-V wafers
  2", 3", 4"

- Processing of SOI wafers
  8" or 12"
  (modulators, detectors, passive waveguides, etc.)

- III-V die or wafer bonding on processed SOI

- InP substrate removal

- III-V patterning
  Heterostructure
  Mesa

- Final BEOL, 2 levels, CMOS compatible, planar

- Laser “passives”
200mm Technological Platform III-V (Laser) Add-on

Laser BEOL evolution “CMOS compatible” and low R (10Ω → 5Ω)

Rserie: TRX2 [4Ω-6.5Ω]
Mean 4.95 Ω
A toolbox for High Performance Computing (1)

Leti’s photonic assisted many-core processor demonstrator

21/10/2018
# Interconnect solutions for Interposers

## Metallic interposer
- **Pro’s**
  - No FEOL: high yield, low cost
  - Low latency
- **Con’s**
  - Point-to-point lines, bad scaling with nb. Cores for area & power
  - Low bandwidth density due to shielding & spacing

## Active interposer
- **Pro’s**
  - Routing logic (NoC)
  - Legacy peripherals
- **Con’s**
  - High synchronous latency
  - Low energy efficiency
  - Many metal layers needed for bandwidth density
  - Older technology for yield

## Optical interposer
- **Pro’s**
  - Low latency
  - High bandwidth density, even more with WDM
  - Possible multiple access
- **Con’s**
  - Static power (requires high utilization)
Optical Network on Chip for Many core processors

- Photonic assisted processor

Integration for high performance:
- Scale-out
- Many-core architecture

Chiplet for low cost:
- Small to medium size chips (1 cm² max)
- Advanced technology node
- Generic
- High volume

Scalable computing component

Interposer for specialization:
- System-in-Package, Silicon (Passive or active), photonic
- Heterogeneous integration enablement
- Application specific

Chipllet concept
Memory proximity – high bandwidth
Optical Network on Chip for Many core processors

Ring/Bus topology

\[ \lambda_0, \lambda_1, \lambda_2, \lambda_3 \]

PN rings for Tx tuning

Photodiodes for Rx data & tuning

PIN rings for Rx

Chiplet 0

Chiplet 1

Chiplet 2

Chiplet 3

Chiplet 4

Chiplet 5

Chiplet 6

Chiplet 7


2018 PIC International Conference, Brussels, Belgium | Yvain Thonnart | April 11th 2018
Design targets

• Ultra-dense integration
  – Full optical connection between all transceivers
  ➜ Drivers < 3D connection interface pitch to the photonic interposer (~0.01mm² per channel)

• Wide temperature range
  – Dissipated power in manycores ➜ temperature rises up to TDP of the package,
  ➜ 0°C to 90°C operating range
1st Gen. EIC and PIC

- Functional area
  - Heater control
  - $40 \times 40 \mu m^2 / \lambda$
  - $40 \times 40 \mu m^2 / WDM$
  - Tx Driver
  - $80 \times 40 \mu m^2$
- Dominated by
  - 6 Cu-Pillar area
  - Pitch $40 \mu m$
  - 2 for Modulator
  - 2 for Photodiode
  - 2 for Heater

TIA w. tuning
& 50Ω output buffers

Tx w. tuning

TIA+Rx w. tuning
1st Gen. EIC and PIC
Results Highlight

• Demonstration of a 3D-stacked CMOS-on-Si-photonic 10Gbps transceiver chip for thermally robust short-range optical communication
  – Wavelength locking achieved in 120μs
  – Stability maintained under 1kHz environmental fluctuation
  – Total CMOS footprint for drivers is 0.01mm$^2$ per channel for up to 1Tbps/mm$^2$ communication density

• Proposal of an all-to-all optical network on chip architecture on interposer for high-density optical communication in high-performance computing systems
  – Scalable intricated-spirals topology with a single waveguide per node
  – No waveguide crossings
  – Invariant CMOS / Photonic interface for tileable chiplets on interposers
A toolbox for High Performance Computing (2)

Other demonstrators

21/10/2018
Other photonic interposer realisations

- **IRIS**
  12λ, 4 Ports, 8 A/D ports

824 Heater controls + 84 TIAs

S. Tondini, OFC2018
Other photonic interposer realisations

Hewlett Packard Enterprise

A. Seyedi European 3D summit 2018
A toolbox for High Performance Computing (3)

Future Developments

21/10/2018
3D integrated many core photonic assisted processor

- Face-to-face microbumps
- TSV in photonic die
- Back-side RDL
- On-chip laser (III-V integration)

- Denser integration
- Higher scalability
- Lower power consumption

Kevin Morot,
Intégration et modélisation RF des interconnexions 3D pour l’interposeur photonique,
PhD dissertation
Packet Switched ONoC

Use Double rings to improve bandwidth density

4x4 single \(\lambda\) switch with double rings

Fractal-like architecture to build \(NxN\) switch with \(M\) \(\lambda\)
Conclusions

• Silicon photonics toolbox developed in 200mm platform
  – Standard passive and active devices (modulators, photodetectors, etc…)
  – SiN layer for additional networking functionality and easier optical assembly
  – TSV for dense integration and scalability
  – Laser integration for ultimate integration step
  – Transfer on 300mm industrial platform (STm)

• Several ONoC projects have been conducted
  – WDM enabled
  – Ring modulators as ultra-dense modulation devices and filters
  – Robust thermal control demonstrated
  – Optical switching function in progress

• Future steps:
  – Full multicore processor on a single interposer
  – Optically Switched NoC
Merci de votre attention