DESIGNING LARGE-SCALE PHOTONIC INTEGRATED CIRCUITS (PICs)

Muhammad Umar Khan, Yufei Xing and Wim Bogaerts
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OUTLINE

• Large scale PICs
  • Fabrication imperfections/variability
    • Silicon-on-insulator (SOI) waveguide

• Design flow
  • Layout aware yield prediction
    • Parameter Extraction & spatial variability

• Summary
PHOTONIC LARGE-SCALE INTEGRATION IS HERE

Photonic switch
Cheng, et al., Optics Express 2018

32 × 32 SiPh switch matrix
D. Celo et al. 2016

Quantum silicon chip
J. Wang, et al. Science 2018
PHOTONIC LARGE-SCALE INTEGRATION IS HERE

• Large scale PICs
  • Complexity
  • Functionality 😊

• Fabrication imperfections
  • Linewidth and thickness
    • Not as desired 😞
  • Fabrication variations accumulate
    • Performance degradation 😞
  • Lower fabrication yield
    • Expensive 😞
FABRICATION IMPERFECTIONS (VARIABILITY)
SILICON PHOTONIC WAVEGUIDE

\[ n_1 (= 3.5) > n_2 (= 1.45) \]

Si substrate

silicon-oxide

silicon

200 nm

500 nm

200 nm
DIMENSIONAL DEPENDENCE OF A WAVEGUIDE

Effective index for different widths

Effective index for different heights
SENSITIVITY OF SILICON PHOTONICS

Silicon photonic waveguides are sensitive to

- geometry
- stress
- temperature
- …

\[
\frac{\partial \lambda}{\partial w} \approx 1 \text{ nm/nm}
\]

\[
\frac{\partial \lambda}{\partial h} \approx 2 \text{ nm/nm}
\]

\[
\frac{\partial \lambda}{\partial T} \approx 0.08 \text{ nm/K}
\]

where 

1 nm \approx 10 \text{ K}

1 nm \approx 20 \text{ K
**Sources of Non-uniformity**

- **Reticle/Mask**
  - CD uniformity
  - Flatness
  - Transmission

- **Litho tool**
  - Exposure dose
  - Slit uniformity
  - Chuck flatness
  - Focus stability
  - Scan direction
  - Source spectrum

- **Resist process**
  - BARC uniformity
  - Resist uniformity
  - PEB °C Uniformity
  - Developer
  - Metrology

- **Wafer**
  - Wafer flatness
  - Stack uniformity
  - Topography

- **Etch process**
  - Plasma Chemistry
  - Coil power stability
  - Bias stability
  - Resist coverage
  - °C stability
  - Metrology
VARIABILITY EFFECTS WORK ON DIFFERENT SCALES

intra-die

distance

intra-wafer (die-to-die)

wafer-to-wafer

lot-to-lot

time
**Describing Variability at Different Levels**

**Process Conditions**
- Exposure dose
- Resist age
- Plasma density
- Slurry composition

**Device Geometry**
- Line width
- Layer thickness
- Sidewall angle
- Doping profile

**Optical Device Properties**
- Effective index
- Group index
- Coupling coefficients
- Center wavelength

**Circuit Properties**
- Optical delay
- Path imbalance
- Tuning curve

**System Performance**
- Insertion loss
- Crosstalk
- Noise figures
- Power consumption
DESIGN WORKFLOW

• Parameter Extraction & Spatial Variability
  • Geometrical parameters
    • Waveguide width
    • Waveguide thickness
      • Optical parameters
      • Mapping of optical parameters to geometrical parameters

• Layout-Aware Yield Prediction
PARAMETER EXTRACTION & SPATIAL VARIABILITY
PARAMETER EXTRACTION

• Metrology measurements
  • Scanning electron microscope (SEM)
  • Atomic force microscope (AFM)
    • Time consuming 😞
    • Expensive 😞
    • Destructive 😞
    • Extraction error (~nm) 😞
    • Few places on the wafer/die 😞

• Optical Measurements
  • Fitting of measurements to simulations
  • Mapping of optical parameters to geometric parameters
    • Smaller extraction errors (sub-nanometer) 😊
    • Non-destructive 😊
    • Many places over the wafer/die 😊
• Extract parameters \( (n_{\text{eff}}, n_g) \) using wafer scale measurements
• Link \( n_{\text{eff}}, n_g \) to width and thickness
• Cannot separate straight and bend waveguide

Lu, Optics Express 2017
EXTRACTION - OPTICAL MEASUREMENTS OF TWO MZIs

Low order
- Inaccurate extraction
- Tolerant to overall variation
- Set reference effective index

High order
- Accurate extraction of group index and effective index

Low order MZI

$\Delta L$

High order MZI

$m \cdot \lambda_{res} = n_{eff} \cdot \Delta L$

$n_g = \frac{\lambda_{res}^2}{FSR \cdot \Delta L}$

Spectrum
- $n_{eff}, n_g$: Straight waveguide
- Length difference between two arms
MEASUREMENT SITES

$$m \cdot \lambda_{res} = n_{eff} \cdot \Delta L$$

$$n_g = \frac{\lambda^2_{res}}{FSR \cdot \Delta L}$$

25 dies
44 copies of MZI pairs per die

$$(n_{eff}(\lambda_0), n_g(\lambda_0)) \rightarrow (w, t)$$

Samples layout
44 copies of MZIs
\[ \Rightarrow n_{\text{eff}}, n_g \]
**DIRECTIONAL COUPLERS**

Treat coupler as circuit:

- 4 waveguides with their sensitivity to $w, t$
- 1 logical coupler with sensitivity to $w, t$

Coupling model = dispersive: straight + bends

Sensitivity calculated using mode solver + FDTD

\[ K = \cos^2 (\kappa_0 + \kappa' L) \]

\[ \kappa_0(\lambda) = \kappa_0(\lambda_0) + \frac{\partial \kappa_0}{\partial \lambda} (\lambda - \lambda_0) + \frac{1}{2} \frac{\partial^2 \kappa_0}{\partial \lambda^2} (\lambda - \lambda_0) \]

\[ \kappa'(\lambda) = \kappa'(\lambda_0) + \frac{\partial \kappa'}{\partial \lambda} (\lambda - \lambda_0) + \frac{1}{2} \frac{\partial^2 \kappa'}{\partial \lambda^2} (\lambda - \lambda_0) \]
**WORKFLOW TO EXTRACT GEOMETRY PARAMETERS**

Extraction error of this experiment

Width: 0.37 nm

Thickness: 0.26 nm

Match optical measurement with circuit simulation to extract behavior parameters

\[ n_{eff}(\lambda_0), n_g(\lambda_0), \ldots \]

Obtain geometry parameters

\[ \left(n_{eff}(\lambda_0), n_g(\lambda_0)\right) \xrightarrow{(w,t)=f\left(n_{eff}(\lambda_0), n_g(\lambda_0)\right)} (w,t) \]

Xing et al., Photonics Research 2018
SYSTEMATIC INTRA-DIE VARIATION

Xing et al., GFP 2018
SYSTEMATIC INTRA-WAFER VARIATION
LAYOUT-AWARE YIELD PREDICTION
YIELD PREDICTION SCHEME

- **PDK + sensitivity**
- **Building blocks + models**
- **Circuit netlist + layout**
- **Sensitivity of model parameters to fabrication parameters** \( \frac{\partial n_{eff}}{\partial w} \), ...
- **Wafer maps (or model) for fabrication parameters**
- **Place circuit on wafer and adjust model parameters**
- **Monte-Carlo on dies and wafers**
- **Yield prediction**

**Circuit Simulation**

**Variability**
- **Pass**
- **Reject**

**Transmission [dB]**

- **wavelength**
  - 1.530
  - 1.535
  - 1.540
  - 1.545
  - 1.550
  - 1.555
  - 1.560
  - 1.565
  - 1.570

**crosstalk**
**Example: MZI Lattice Filter**

Simple (but sensitive) building blocks

- directional couplers
- waveguide delay lines

FSR = 800GHz (~6.4nm)

Pass-band = 80GHz

Guard band = 80GHz

Crosstalk (rejection) = -15dB

Center wavelength = 1.55μm

Long directional couplers

- dispersive
- very sensitive
**Wafer Maps: Width and Thickness**

Most straightforward parameters

- Linewidth map
  - Simplex noise model
    - \( radius = 200\mu m \)
    - \( amplitude = 1\text{nm} \)

- Thickness map (measured)
  - \( range = 213 - 219\text{nm} \)

*Bogaerts et al., JSTQE 2019*
**Sampling Points in the Layout**

All building blocks with a model will sample all variables \((w, t)\)

- waveguides: \(n_{eff}, n_g\)

- logical couplers: \(\kappa', \frac{\partial \kappa'}{\partial \lambda}, \frac{\partial^2 \kappa'}{\partial \lambda^2}, \kappa_0, \frac{\partial \kappa_0}{\partial \lambda}, \frac{\partial^2 \kappa_0}{\partial \lambda^2}\)

- Sampling points are aggregated over the component: results in averaging, same as in fabricated devices
Monte-Carlo Simulations Over a Wafer

10mm spacing

277 dies on a wafer

Using CAPHE circuit simulator (Luceda)

1000 wavelength points
YIELD MAPS

Without absolute wavelength spec

With absolute wavelength spec:
peak = 1.55μm ± 80 GHz
PEAK WAVELENGTH: LARGELY AFFECTED BY THICKNESS

Wafer thickness map

yield on wavelength spec
**IMPROVE FILTER?**

Sweep number of taps

- More taps: better (box-like) filter
  - higher rejection ratio
  - sharper edges
- With variability
  - phase errors add up
  - coupler errors add up

![Diagram](image)
**Yield Analysis**

Increase number of taps:

- **2**: not enough taps to reach rejection ratio
- **4-8**: good quality
- **10-14**: variability kills performance

*Best: 6 taps*

Yield specifications:
- \( \Delta \lambda_{\text{peak}} < 40 \text{GHz} \mu\text{m} \)
- Rejection < \(-15\) dB
- Pass band ripple < 1 dB
- Transmission > 1 dB

![Graph showing yield vs. number of couplers]

- Good devices with too large wavelength offset
- Good devices with acceptable wavelength offset

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*Image credit: Ghent University - imec*
SUMMARY

• Fabrication Imperfections
  • Variability

• Variability determines yield in large circuits
  • Variability should be considered at design stage

• Need layout awareness for yield prediction
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http://epixfab.eu/trainings/upcoming-trainings/spdc19/