THERMALLY-TUNED PHOTONIC LINKS TOWARD OPTICAL NETWORKS ON INTERPOSER
Silicon Photonics moves forward for long distance optical wireline transceiver
• 100 / 400 Gigabit Ethernet

Large-scale electronics longs for low-latency low-energy dense communication

Optical short-range communication has been a long-term target for years
• Needs compact optical devices to maximize bandwidth per mm² ➔ Microring optical resonators
Microrings & Photodiodes are compact & fast
• Area $< 100\mu m \times 100\mu m$ – Bandwidth $> 10$ GHz

Waveguides have low latency & low losses
• Propagation $\sim 10$ cm/ns – Losses $\sim 0.1$ dB/cm

But Chip activity creates temperature changes $\Rightarrow$ disturbs the microrings
Experiment: 4Gbps modulation under laser wavelength wobulation 30pm_{pp} at 100Hz

Simulate thermal effect of workload changes on package (~1-10ms time constant)

CIRCUIT OBJECTIVE: PRESERVE COMMUNICATION DESPITE ENVIRONMENTAL PERTURBATION

No wobulation

Wob+Thermal tuning deactivated

Wob.+Thermal tuning activated
Context: Silicon photonics for short-range communication

Silicon-photonic devices

Closed-loop analog tuning & WDM remapping

TOWARD demonstrator

Measurements & benchmarking
Compact optical devices

- Highly resonant: Q-factor 10,000–30,000

Any refractive index change shifts the resonant wavelength

PN or PIN diode junction can be created inside the ring for electrical control

- Different uses depending on diode
  - PN rings can be used as modulators (> 10 Gbps)
  - PIN rings can be used as filters (<500 MHz) for routing and wavelength demultiplexing

But Subject to Temperature variations

⇒ Low-frequency resonance shift

\[ \lambda_{res} = \frac{P n_{eff}}{k} \]
MODULATOR PRINCIPLE, THERMAL SENSITIVITY DA/DV & DΛ/DT MEASUREMENTS

13.6 pm/V modulation efficiency

76 pm/K thermal sensitivity

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Heating using doped Silicon
• Resistive path inside the ring

Average ring temperature increase:
• Simulation: \( \frac{dT}{dP} \sim 2K/mW \)
• Measurements: \( \frac{d\lambda}{dP} \sim 40\text{pm/mW} \)

70nm Silicon film to preserve electrical connectivity for modulation

Could be improved by 10×
• Ti heater
• Back-side selective substrate removal
Optical measurements
- square wave on heater
- Test probes on Photonic die

Exhibits a 2nd order response
- distorsted due to lorentzian λ response
- local heating around 4μs
- heat diffusion around 25μs

Response modeled as a laplace transform
- Heat diffusion: dominant pole at 25μs
- Local heating: zero at 5μs, secondary pole at 2μs

\[ H(s) = k \cdot \frac{1 + 5\mu s \cdot s}{(1 + 25\mu s \cdot s)(1 + 2\mu s \cdot s)} \]
Ring resonant wavelength unpredictable at design time
- 1 nm thickness variation
  \( \approx 1 \text{ nm resonance shift} \)

But finesse, free-spectral-range & amplitudes are well-controlled

Thermal tuning is used to align ring resonance on laser source
- Low-frequency control

Voltage is used to modulate light
- High frequency modulation
When total data throughput is sufficient: use several wavelengths

- Reduces the required shift for thermal tuning
  - From at most 1 FSR to at most 1/n FSR
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Measurements & benchmarking
Ring resonance can be tracked by transmission on drop port

- Setpoint on through port corresponds to a power value on drop port
- Photodiode converts this to photocurrent
- Analog control used to match photocurrent with reference
- Joule heating by resulting heater driver current
Track heater command for minimum and maximum heating
  • Allow for 20% overlap

When overheat is reached
  • better switch to a higher wavelength ➔ Cool down
& Vice-versa for underheat

Use analog comparators on heater voltage
Peak edges have different signs for dP/dT

- One side is stable and the other is not

Swapping signal & reference in control loop allows switching stable edges

- Increasing/decreasing the reference allows leaving metastable state

Transition from one peak to another done in two steps

- Ring is never driven in open-loop
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Measurements & benchmarking
ELECTRONIC DIE, PHOTONIC DIE & ASSEMBLY

TIA w. tuning
& 50Ω output buffers

Tx w. tuning

TIA+Rx w. tuning

Functional area
• Heater control
• 40×40μm²/λ
• 40×40μm²/WDM
• Tx Driver
• 40×40μm²
• Rx Driver
• 80×40μm²

Dominated by 6 Cu-Pillar area
• Pitch 40μm
• 2 for Modulator
• 2 for Photodiode
• 2 for Heater

DC supplies & config. wirebonding

Fiber array

Level RF CoB wirebonding

Ring & photodiode

Grating coupler array

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**Experimental Setup**

- **Optics Workshop**
  - Date: 2018
  - Yvain Thonnart

**DC Configuration**
-+=

- **Tunable-wavelength Laser Source**
- **LF Laser Wavelength Controller**
- **RF PRBS @10Gbps**
- **DC Config. Laptop**
- **CMOS+SiPho DUT**
- **Ext. Optical Modulator**
- **Oscilloscope LF Optical Monitoring**
- **RF Oscilloscope/Analyzer**
- **Eye Diagram**
- **Tuning Monitoring**

**Simulate Environmental Variations**

**In/Out Fiber Array**
- **DUT Under Fiber Array Probe**
- **In/Out RF Signals**
- **RF In/Out**
- **Laser**
- **LF Monitoring**

**RF PRBS**

**Thresholds**, tgt. optical power…

**DC Configuration Board**

**In/Out Fiber Array**

To laser sources & optical scope
Context: Silicon photonics for short-range communication

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TOWARD demonstrator

Measurements & benchmarking
THERMAL TUNING WITH LAMBDA SWEEP

Optical power (A.U.)
Laser wavelength (nm), increasing λ sweep at 1nm/s

Heater lock during λ sweep

Reference power configuration
chip off
0 (running, cold)
10
20
31
44
63 (max heat)

Ref. power too high

Laser wavelength (nm), increasing λ sweep at 1nm/s

Heater Joule Power (μW)

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Wavelength locking on reference level on thermal control activation / remapping

- Off-resonance
- 100μs lock-time
- Near-resonance @-3dB

Thermal control stability under 30pmpp wavelength wobulation

- Off-resonance
- Disabled @900Hz
- Enabled @900Hz
- Res-peak @mod off

Pheat=0.4mW
ROBUST ELECTRO-OPTICAL LINK OPERATION UNDER PERTURBATION

END-TO-END COMMUNICATION: RX AND TX RINGS TUNED TO THE SAME WAVELENGTH
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Integration scheme</td>
<td>3D face-to-face</td>
<td>2D proximity wirebonding</td>
<td>Monolithic</td>
<td>3D face-to-face</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm SOI SiPh 40nm CMOS</td>
<td>130nm SOI SiPh 65nm CMOS</td>
<td>45nm CMOS SOI</td>
<td>100nm SOI SiPh 65nm CMOS</td>
</tr>
<tr>
<td>Datarate</td>
<td>20 Gbps</td>
<td>24 Gbps</td>
<td>10 Gbps</td>
<td>10 Gbps</td>
</tr>
<tr>
<td>Ring Q factor</td>
<td>~5500</td>
<td>~5000 Tx, ~18000 Rx</td>
<td>~11600</td>
<td>~30000</td>
</tr>
<tr>
<td>Wavelength</td>
<td>1550nm</td>
<td>1550nm</td>
<td>1180nm</td>
<td>1310nm</td>
</tr>
<tr>
<td>WDM channels</td>
<td>4</td>
<td>5</td>
<td>11</td>
<td>4</td>
</tr>
<tr>
<td>Thermal tuning</td>
<td>Open-loop</td>
<td>Digital closed-loop avg/peak det.</td>
<td>Digital closed-loop bit-statistical (Tx only)</td>
<td>Analog closed-loop with digital reconfiguration</td>
</tr>
<tr>
<td>Wavelength remapping</td>
<td>No / External</td>
<td>No / External</td>
<td>No / External</td>
<td>Integrated &lt;1ms remap time*</td>
</tr>
<tr>
<td>Heater efficiency</td>
<td>0.16nm/mW</td>
<td>0.16nm/mW</td>
<td>1.25nm/mW</td>
<td>0.04nm/mW</td>
</tr>
<tr>
<td>Tuning ctrl. power</td>
<td>N.A. – External</td>
<td>170μW</td>
<td>720μW</td>
<td>150μW</td>
</tr>
<tr>
<td>Tuning precision</td>
<td>N.A. – External</td>
<td>Not reported</td>
<td>5pm</td>
<td>0.5pm</td>
</tr>
<tr>
<td>Tuning lock-time</td>
<td>N.A. – External</td>
<td>700ms</td>
<td>6.7ms</td>
<td>120μs</td>
</tr>
<tr>
<td>Tuning bandwidth</td>
<td>N.A. – External</td>
<td>~1Hz (from transient meas.)</td>
<td>~1Hz (from transient meas.)</td>
<td>900Hz</td>
</tr>
<tr>
<td>Tuning area / ring</td>
<td>0.04mm² (pad area)</td>
<td>0.03mm²</td>
<td>0.0024mm²</td>
<td>0.0016mm²</td>
</tr>
<tr>
<td>Tot. driver area / λ</td>
<td>0.14mm² (Tx or Rx)</td>
<td>0.1 / 0.06 mm²(Tx / Rx)</td>
<td>0.0205mm² (Tx)</td>
<td>0.0096mm² (Tx or Rx)</td>
</tr>
<tr>
<td>Bandwidth density</td>
<td>142 Gbps/mm²</td>
<td>300 Gbps/mm²</td>
<td>391 Gbps/mm²</td>
<td>1 Tbps/mm²</td>
</tr>
</tbody>
</table>

* Remapping simulated for heater efficiency of 1.25nm/mW (not attained due to lack of selective substrate removal as in [5])
3D-stacked CMOS-on-Si-photonic 10Gbps transceiver chip for short-range optical communication

• Focus given on digitally-supervised analog wavelength stabilization and remapping using microring heaters
• Wavelength locking on a constant wavelength achieved in 120μs
• Stability of the tuning is maintained under 900Hz environmental fluctuation.
• Total CMOS footprint for control and drivers is 0.01mm² per microring for up to 1Tbps/mm² communication density.
Thank you!

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