Opportunities and Obstacles of Monolithic III-V Integration on Silicon

Y. Léger, C. Cornet, R. Tremblay, A. Létoublon

UMR FOTON, CNRS, INSA Rennes, Université de Rennes 1, Enssat, F35708, Rennes, France
Cisco Trends:
- The amount of VoD traffic in 2020 will be equivalent to 7.2 billion DVDs per month.
- Virtual reality traffic quadrupled in 2015
- The number of devices connected to IP networks will be more than three times the global population by 2020

Energy sustainability
- Heat losses in datacenters
- Heat losses in smartphones and computers
Towards 3D hybrid microprocessors

3D electronic architectures
Substrate removal integration
(coming from GPU)

MIT Lincoln lab (2013)

Hardware and functional hybridization

- different functionalities (memory, routing, computing)
- different technologies (photonic?)
- different computation paradigms

Integrated lasers on Silicon, Elsevier 2016
State of the art of photonic building blocks

- on-chip optical waveguides for visible and IR wavelengths
- detectors
- modulators
- advanced components (filters, AWG etc...)
- on chip lasers

III-V is the only mature laser platform

Xiophotonics.com
Wafer bonding

Fastest time to market?

**Full wafers**
Scalability issue
Gas by-products evacuation

**Small die bonding**
Reproducibility

**Massive transfer Printing**
III-V coupons on Stamps
Scalability and accurate positioning

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Luo et al. Front. Mater. 2015

CEA-Leti

B. Corbett's group

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Foton
Monolithic integration: direct growth of III-V on Si

Cheaper, Straightforward scalability
But can it be mature?

- Polar on non-polar crystals
- Lattice mismatch

![Diagram showing III-V (zinc Blende) and Silicon (diamond cubic)]
### Surface preparation

- Defects induced by pollution of the substrates
- Advanced substrate preparation
- Microtwins: rotations of the III-V crystal
- No optoelectronic characterization

- Huge roughness
- Not the only problem

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### 3D nucleation

STM of the nucleation layer

Cross TEM after 100nm of non-managed growth

Antiphase domains

- bi-stepped surface -> vicinal substrates
- Initial Ga or P coverage

Annihilation layers

- GaP/Si
- Al-Rich layers to control the annihilation height

Wafer preparation

- LTM
- GaAs/Si
- Vicinal to nominal

Alcotte et al. APL Mater. 2016
Polar on non-polar defects

**Antiphase domains opto-electronic impact**

- **Electric shunts**

![Graph showing voltage vs. intensity](image)

- **Induced absorption**

![Graph showing energy vs. log(ε/ε₀)](image)

*Tea et al. J. Appl. Phys. 2014*

- **Interesting for nonlinear optics**

Optics Workshop, DATE 2017
Lattice mismatch

- pseudomorphic and metamorphic growth

GaP/Si emitters
- QDs 100nm above Si interface
- room temperature emission

Huge advances on GaAs/Si devices!
GaAs metamorphic integration

Threading dislocation management

- Strained layer Superlattice
- Requires a thick buffer
- Lifetime issue

CMOS compatible design

- Laser
- 2.7 \( \mu \)m Pseudo substrate

Strained layer Superlattice
- Requires a thick buffer
- Lifetime issue


Chen et al. Opt. Express 2017

Optics Workshop, DATE 2017

2017-03-31
GaAs/Si laser performances

- Large temperature span
- State-of-the-art thresholds
- Long lifetime

**On nominal 300mm Si**

*Chen et al. Opt. Express 2017*

**On vicinal Si**

*Chen et al. Nature Phot. 2016*
Defect management for III-V/Si integration becomes mature

GaAs/Si lasers reach state-of-the-art performances
- smaller consumption than InP-based lasers
- Si transparency emission
- promising lifetimes

Remaining issue of the pseudo-substrate
- Interest of SOI integration?
- 3D integration (substrate removal)
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