SCALING UP SILICON PHOTONICS: WHERE ARE THE CHALLENGES

Wim Bogaerts

OPTICS2017 Workshop, Lausanne, 31 March 2017
THE PHOTONICS RESEARCH GROUP

Research Group of Ghent University
- within Engineering Faculty
- within Dept. of Information Technology (INTEC)
- associated with IMEC
- member of NB Photonics

8 Professors (5 ERC grantees)
16 postdocs
50 PhD students
10 support staff
1 Business developer
15 nationalities
WHAT IS SILICON PHOTONICS?

The implementation of high density photonic integrated circuits by means of CMOS process technology in a CMOS fab

Enabling complex optical functionality on a compact chip at low cost

Pictures, courtesy of imec
THE PAST 15 YEARS: STUNNING RESEARCH PROGRESS

Citation Report: 8566
(from Web of Science Core Collection)

PUBLICATIONS EACH YEAR

Start of industrial interest

(Conferences not included)
INDUSTRIAL TAKE-UP EXAMPLES IN TELECOM/DATACOM/DATA CENTERS

• active optical cables (eg PSM4: 4x28 Gb/s on parallel fibers)
• WDM transceivers (eg 4 WDM channels x 25 Gb/s on single fiber)
• coherent receiver (eg 100 Gb/s PM-QPSK)
• fiber-to-the-home bidirectional transceiver (eg 12 x 2.5 Gb/s)
• monolithic receiver (eg 16x20Gb/s)
• 40Gb/s, 50Gb/s and 100 Gb/s Ethernet (future: 400Gb/s)
• ...
Why Silicon Photonics?

Large scale manufacturing

Scale

Submicron-scale waveguides
WAVEGUIDES: SILICON PHOTONIC WIRES

High index contrast waveguides

- submicrometer dimensions
- small bend radius
- high-density photonics (> 10000 components/chip)

![Waveguide diagram]

Silicon-oxide

Si substrate

Optical mode
HIGH INDEX CONTRAST: A BLESSING AND A CURSE

Every nm$^3$ matters

CMOS technology is the only manufacturing technology with sufficient nm-process control to take advantage of the blessing without suffering from the curse.
VARY LARGE SCALE (INTEGRATION)

TSMC Fab 14
1.4M 300mm wafers / year

Source: TSMC
ECONOMY OF (WAFER) SCALE

Wafer-scale economics

- Larger wafers
- Higher volumes
- Massive parallelism
- Minimal marginal cost

- More expensive tools
- Higher volumes
- Larger fixed cost
ECONOMY OF (WAFER) SCALE

Chip cost per mm² in a dedicated, loaded fab.

Strong function of volume

Source: JePPIX Roadmap 2015
ECONOMY OF (WAFER) SCALE

Chip cost per mm$^2$ in a dedicated, loaded fab.

Source: JePPIX Roadmap 2015
ECONOMY OF (WAFER) SCALE

Chip cost per mm$^2$ in a dedicated, loaded fab.

Source: JePPIX Roadmap 2015
A SHARED FAB?

CMOS Fab making both CMOS and silicon photonics

- CapEx for CMOS fabrication fully recovered (= old fab)
- Fab should have some (variable) spare capacity

Technological capabilities required?

- preferably 300mm (better wafers)
- 65-90nm CMOS node
- Upgrade with Germanium epi
- Upgrade with better lithography
THE DRIVE FOR SILICON PHOTONICS: OPTICAL INTERCONNECTS

Optical communication has
- higher bandwidth
- lower propagation loss

Optical interconnects are shrinking
• Data center
• Rack-level
• Board-level
• Package level
...
WHAT IS HIGH VOLUME?

Saturated 200mm fab

- $5 \times 5 \text{ mm}^2$ per chip
- 1,250 chips / wafer (200mm)
- 40,000 wafers / month
- 50 Mchips / month
WHAT IS HIGH VOLUME?

**Saturated 200mm fab**

5×5 mm² per chip

1,250 chips / wafer (200mm)

40,000 wafers / month

50 Mchips / month

2018

~1 fabmonth

**Datacenter Cabling**

50 mega datacenters

10,000 racks / center

64 cables / rack

2 transceivers per cable

64 Mchips

2022

<2 fabyears

**Datacenter Cabling**

50 mega datacenters

10,000 racks / center

1,000 cables / rack

2 transceivers per cable

1 Gchips
Silicon Photonics: only for interconnects?

Transistors: only for calculators?
WHEN DOES THIS FUNCTIONALITY/COST MAKE SENSE?

Large Volume
• millions of chips
• high yield
• low cost

High complexity
• thousands of functions on a chip
• large-scale integration
• high cost
• yield?
**Bio & Gas Sensors**

- Silicon photonics: cheap disposable sensor
- Needs transducer to translate the presence of particular molecules into a refractive index change
- Mostly work on the chemistry/material science side

![Diagram showing the components of a silicon photonics sensor chip, including input grating coupler, sensor element, fluid channel, output grating coupler array, and 128 sensors on a chip.]
COMPACT SWITCH MATRICES

32 x 32 switch matrix on a 12 x 12 mm² chip
SPECTROSCOPIC SENSORS SYSTEMS

E.g. Integrated glucose monitoring

- 4 spectrometers in 4 wavelength regions
- measure clinically relevant glucose concentrations in biological fluids
**LARGE PHASED ARRAYS**

Large arrays of optical “antennas”
Individual phase/amplitude control
Beam steering & forming

![Image of large phased array](image-url)
SILICON PHOTONICS AND CMOS

The **STRENGTH** of Silicon Photonics is that it can make use of CMOS-technology.

The **WEAKNESS** of Silicon Photonics is that it **must** make use of CMOS-technology.

CMOS-technology requires insanely expensive infrastructure but delivers ridiculously cheap chips with a ludicrous degree of sophistication.
**WHO OWNS A FAB FOR SILICON PHOTONICS?**

**Vertically integrated electronics manufacturers**
- high-end or specialty electronics (e.g. INTEL, ST)
- Silicon Photonics for own use or select partners

**CMOS Foundries** (TSMC, Global, Silterra, …)
- commodity electronics processes in high volumes
- Silicon photonics for industrial customers
- Need sufficient volume to warrant upfront cost

**Research Fabs**
- Already running silicon photonics (IMEC, LETI, IME, IHP, CNSE, …)
- Prototyping services and Multi-project-wafer shuttles
- No capacity or interest in larger volumes?
TECHNOLOGY PLATFORMS FOR SILICON PHOTONICS

R&D and prototyping platforms:

- Imec, Belgium (MPW-service through ePIXfab / Europractice)
- CEA-LETI, France (MPW-service through Europractice/CMP)
- VTT, Finland (“thick SOI”)
- IME, Singapore (MPW-service)
- AIM-Photonics, USA (MPW service starting 2016)
- AIST (MPW service planned in 2018)

Manufacturing platforms:

- Freescale
- ST Microelectronics
- IBM
- Intel
- GlobalFoundries
- TowerJazz
MULTI-PROJECT-WAFER (MPW) SERVICE

The “reticle” (= basic unit that is repetitively patterned on the wafer) has a maximum size of \(~25 \times 25\) mm.

That equals 25 times a \(5 \times 5\) mm chip.

On a \(200 \) (300) mm wafer you can fit 50 (110) full fields.

So, let’s get organized.

1. Collect 25 \(5\times5\) mm designs from different users.
2. Combine these designs on a single mask set.
3. Collectively process the wafers (typically 25 wafers in one batch).
4. Dice the wafers down to \(5\times5\) mm chips (!!).
5. Send a few dozens of \(5\times5\) mm chips to each user, together with an invoice.
FABLESS SILICON PHOTONICS

Many fabless Silicon Photonics companies have emerged

• from direct collaboration with fabs (Luxtera, ...)
• starting from MPW (Caliopa, Genalyte, Acacia)

Established players are also partnering

• e.g. Finisar with ST
• Many keep their fab a secret

How to enter as a new (fabless) startup?
**Silicon Photonics: From Idea to Product**

What if you do not have a fab?

**Test your idea**
- prototype in your own clean room
- rapid iteration cycles

**Low volume sampling**
- Dedicated run in research fab
- Allows qualification testing

**Variational validation**
- MPW in research fabs
- multiple samples
- develop packaging

**High volume production**
- Dedicated run in volume fab
SCALING TO HIGH-VOLUME PRODUCTION

Process transfer from research fab to commercial fab

• match the geometries
• match the performance (including variability)
• match the design kit and models
• migrate the other parts of the supply chain (e.g. assembly)
IMEC SILICON PHOTONICS: FROM R&D PIPELINE TO VOLUME MANUFACTURING

Early Research in imec’s Optical I/O Research Program
Development & Prototyping at imec
  – Limited amount of wafers/year
  – Reliability qualification ongoing
High-Volume Manufacturing at Commercial Foundry
  – imec enables production path at commercial foundry
    – 95% of the flow compatible with CMOS90 technology
FROM SAMPLING TO LOW-VOLUME PRODUCTION

Most Research Fabs (MEC, LETI, IME) offer a LVM model

Low volume (< 1000 wafers / year) can already be enough for first market

Low technology threshold

Potentially high financial threshold (research fabs are expensive per chip)

Potentially long production cycles
FROM PROTOTYPES TO LOW-VOLUME SAMPLING

What you need is
1. a quick turn-around time (rapid learning)
2. run-to-run reproducibility
3. realistic expectation for scaling up

Need to fill this gap
FROM PROTOTYPES TO LOW-VOLUME SAMPLING

Fast prototyping fabs, compatible with MPW fabs

- Fast (days or weeks instead of months)
- Very low volume (1-10 chips)
- Calibrated against an MPW fab
  - Similar processes and specs
  - Similar design flow and design rules
- Consistent quality (monitored process)
- Supported by PDK with models and statistics
- At a similar cost per run
SiP Prototyping Services Are Emerging

IPH, AMO (Germany)
Australia Silicon Photonics
ORC in Southampton (UK)
KIT (Germany)
UBC / UWashington (Canada/US)
Applied NT (Canada)
YOU NEED MORE THAN JUST A FAB

• Design and simulation tools (and services): the supply chain is developing

• Packaging tools: rapid progress but still a long way to go

  New H2020 PIC-packaging project will develop the supply chain
PIC PACKAGING @ TYNDALL
**WHEN DOES THIS FUNCTIONALITY/COST MAKE SENSE?**

**Large Volume**
- millions of chips
- high yield
- low cost

**High complexity**
- thousands of functions on a chip
- large-scale integration
- high cost
- yield?
COMPONENTS PER CHIP

“Moore’s law for Silicon Photonics”

A. Khanna et al. OFC2017, Th1B.3
CONNECTIVITY BEGETS COMPLEXITY BEGETS FUNCTIONALITY

Integrated Electronics

- billions of digital gates: unprecedented logic performance
- millions of analog transistors: unprecedented control
  (even with imperfect components: enabled by design!)

Integrated Photonics (in Silicon)

- **technological potential** of 10000+ photonic elements on a chip
- not even scratched the surface of what this could do

Needs design and control
SCALING COMPLEXITY

Many components on a chip

Scalable building blocks
  • connectivity
  • cascadability
  • variability

Design scaling
  • synthesis tools
  • accurate models
  • yield prediction

Operational scaling
  • control and feedback

10000s optical elements
100s optical IOs
10s RF IOs
10000s optical elements
SCALING COMPLEXITY

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How many devices can we combine in a circuit?

Footprint
Power consumption
Compound losses (or add gain?)
Parasitics and crosstalk

1000s optical elements
10s RF IOs
10000s optical elements
100s optical IOs
1000s electrical control IOs
LOWER LOSSES.

Better technology

- 300mm wafers and tools give better performance
- immersion lithography gives better linewidth control
- lower sidewall roughness reduces loss and backreflection

Other geometries and materials

- rib waveguides
- SiN waveguides
LOSS COMPENSATION

Introduce Gain in silicon photonics

- III-V semiconductors
  - Bonding
  - Epitaxy
- Germanium
- Erbium-doped waveguide amplifiers
- Parametric gain (4-wave mixing)
MODULATORS CONSUME A LOT OF SPACE

Not really in line with ‘submicron’ Silicon Photonics

Alternative phase modulators, tuners and switches?
**Effect Magnitude vs. Speed**

Magnitude of the effect
- Mechanical (ms-us)
  - MEMS, NEMS
- Birefrigence (ms)
  - Liquid crystals
- Thermal (us)
  - Heaters
- Carriers (ns)
  - Diodes, capacitors
- Pockels $\chi(2)$ (fs)
  - Polymers, perovskites

Speed of the effect
- Tuning
- Modulation
- Switching
ALTERNATIVE MODULATOR AND SWITCH TECHNOLOGIES

Modulators

Electro-Optic Polymers in Slot Waveguides
  — Very good performance, but ready as a platform?

Ferro-Electrics on Silicon
  — Pure phase modulation
  — Difficult material integration
  — Recent breakthroughs in loss

Germanium-EA Absorbers
  — Direct intensity modulation, but no phase modulation
  — High speed, low power demonstrated

Graphene on Silicon
  — Direct intensity modulation
  — Much work needed

Switches

Large-Scale MEMS Fabrics
  — Up to 50x50 switch matrices demonstrated
  — Large bandwidth and high XT

Liquid Controlled Adiabatic Switches
  — Towards no static power consumption
  — Broadband low loss operation

Liquid Crystal based switches
PHOTONICS IS JUST ONE PART OF THE SYSTEM

Large-scale photonics requires integrated electronics

- Logic
- Control
INTEGRATION WITH ELECTRONICS: SCALING

Photonics interfaced with electronics

- Monolithic
  - Low parasitics. all-in-one process.
  - Not the optimal process for either.
  - Feature size mismatch
- Flip-chip
  - Large bond-pads, density limited
  - Parasitics
- 3D stacking
  - Best process for both
  - Co-design and yield?

IBM

IMEC
SCALING COMPLEXITY

Many components on a chip
Scalable building blocks
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Design scaling
  • synthesis tools
  • accurate models
  • yield prediction

Operational scaling
  • control and feedback

Automating design
predict the behavior (statistical)
First-time right design
DESIGNING PHOTONIC INTEGRATED CIRCUITS

Can we learn from electronic ICs?

- Millions of analog transistors
- Billions of digital transistors
- Power, timing and yield
- First time right designs

- Very mature Electronic Design Automation (EDA) tools!
- A well established design flow

Does this apply to photonics?
Design Environments are Emerging

Combinations of Photonics Design and EDA

Physical simulation combined with circuit design

Physical and functional verification

First PDKs with basic models
COMPONENT DESIGN VS. CIRCUIT DESIGN

10 years ago: Component Design

- Layout
- Geometry
- Simulation

Now also: Circuit design

- Circuit capture
- Simulation
- Layout
PHOTONIC+ELECTRONIC CIRCUIT SIMULATION

Photonics does not fit in Spice

Effort-flow systems

<table>
<thead>
<tr>
<th>System</th>
<th>Effort (Electrical)</th>
<th>Flow (Mechanical)</th>
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<tbody>
<tr>
<td>Electrical</td>
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<td>Force</td>
<td>Motion</td>
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<tr>
<td>Photonic?</td>
<td>-</td>
<td>-</td>
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</tbody>
</table>

Photonics used other formalisms (more like RF waves)
How much information needs to be exchanged per time step?

- phase?
- spectral information?
- multimode waveguides?
- unidirectional or bidirectional?

*Depends on the application*
SIGNAL REPRESENTATION: EFFECTS CAN BE MODELED

Accuracy

interferometry

Power Phase Wavelength Mode

Power Phase

Power

phase modulation

propagation loss

N channels

Power Phase Wavelength Mode

Power Phase Wavelength Mode

chirp, slow nonlinearities

channel crosstalk

Amount of information needed

Spectrum

Power Phase

GHENT UNIVERSITY
**SIGNAL REPRESENTATION: APPLICATION DESIGN**

- **Accuracy**
  - Power
  - Phase
  - Wavelength
  - Mode

- **Amount of information needed**
  - Power
  - Phase
  - Wavelength
  - Mode

- **N channels**
  - Simple WDM links
  - Coherent links
  - Point-to-point links

- **Spectrum**
  - Spectrometers
  - Power Phase
INTEGRATE PHOTONIC AND ELECTRONIC CIRCUIT SIMULATION

Photonics = Optics + Electronics.
We need to combine the two in the design process.

• Verilog A: Represent Optical Signals as ‘Voltages’ or ‘Power’
• Use busses for power, phase (real/imag) and wavelength
• Cosimulation with Photonic Circuit simulator
PHOTONICS IN VERILOGA

Encode time signals as ‘analytical’ signals (complex numbers)

Bus of two lines for bidirectionality

Modulation on an optical wavelength

C. Sorace-Agaskar, OpEx 23(21), 2015
**Photonic-electronic cosimulation**

Full separation possible?

- In some cases (e.g. link)
- Simulation in one direction
- Exchange waveforms
- No feedback!

**Diagram:**
- Laser
- Waveguide
- Photodiode
- Electrical transmitter
- Optical link
- Electrical receiver
- TIA
FUTURE: MIXED-SIGNAL CO-SIMULATION

2 or more simulators:
- data exchange
- synchronization
- common netlist
- data readout
- ...

Vin

laser

waveguide

optical link

electrical transmitter

tetodio
electrical receiver

TIA

Vout

Vout
CO-SIMULATION

Optical and electrical co-design in Virtuoso Schematic

Photonic simulation in Lumerical Interconnect

A. Farsaei, APC 2016, JTu4A.1
VARIABILITY: PREDICTING CIRCUIT YIELD
**VARIABILITY ≠ VARIABILITY**

Wafer – to – wafer variability

Die – to – die variability

Intra-die variability

- mask-related
- distance related
- stochastic

Thickness map

Linewidth map
DEVICE VARIABILITY ANALYSIS

Standard technique: Monte-Carlo simulations

Requires many expensive simulations

- Device error
  - Fabrication
  - Operation

- Monte-Carlo
  - Simulation
  - Measurement
  - Expensive

- Statistics
  - Standard deviation
  - Probability density
  - Yield prediction

Device Variability Analysis

Build stochastic model from small set of simulations

Use Monte-Carlo on Stochastic model

- Device error
  - Fabrication
  - Operation

- Stochastic model
  - Limited number of Simulation or Measurement

- Monte-Carlo
  - With stochastic model of the device (analytical functions)

- Statistics
  - Standard deviation
  - Probability density
  - Yield prediction
DEVICE VARIABILITY ANALYSIS WITH STOCHASTIC COLLOCATION

- Sampling-based interpolation modelling technique
- Random variables with arbitrary distribution
- Example: variability of directional coupler

<table>
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<tr>
<th>Technique</th>
<th>Mean value of field coupling</th>
<th>Standard Deviation of field coupling</th>
<th>Computational time</th>
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**SCALING COMPLEXITY**

Many components on a chip

Scalable building blocks

• connectivity
• cascadability
• variability

Design scaling

• synthesis tools
• accurate models
• yield prediction

Operational scaling

• control and feedback

Even with today’s technology: Perfection is achievable
Making perfect optics with imperfect components

Replace specialty optical component with a more complex circuit

• Simple building blocks
• (Many) tunable elements
• Simple feedback loops

E.g. Linear N×N circuit
• tunable 2×2 couplers
• tunable delay lines
• monitor detectors

D.A.B. Miller, Optica 2, 747-750 (2015)
PHOTONIC-ELECTRONIC CONTROL ALGORITHMS

Global Algorithms
All system data is available
Less monitors needed
More complex logic -> instabilities?
Less reuse

Local Algorithms
Simple logic, more stable
Reusable in larger circuits
More monitors needed
Limited data available

Chip
Control loop
phase tuners
in
detectors
out
Beam splitters = MZI

IO channels: grating couplers
Phase shifters: Simple Heaters
Power monitors: Directional coupler tap

Ribeiro et al, Optica 2016
**Adaptive Beam Coupler**

Circuit adapts itself to maximize output to a single mode waveguide.

Local feedback loops stabilize the entire circuit.

---

*Feedback on*

*Feedback off*

*Temperature*

---

Ribeiro et al., Optica 2016
MORE THAN JUST PHOTONS

Silicon photonics goes beyond the optical chip

- 100s optical IOs
- 1000s electrical IOs
- 1000s electronic feedback loops
- 10s RF signals
- 10000s optical elements
- Software configuration
PHOTONICS IS JUST ONE PART OF THE SYSTEM

Just good enough photonics technology
Fairly simple silicon photonic circuits (e.g. simple transceiver)
Electronics and software is added to make a system
Existing electronic techniques are used to compensate for photonics
Summary

Economic Scaling in Silicon Photonics
- Based on CMOS fabrication models.
- Large volumes or uniquely large value (complexity)
- New routes emerging for R&D

The only technology to allow complexity scaling (circuit density and connectivity)

Process technology is ‘good enough’ today, but
- Complexity scaling is limited by the design process
- Complexity scaling is limited by the control logic
**Silicon Photonics Design Course**

Gain a deep understanding of the design flow for silicon photonics

- circuit design and simulation
- component design and simulation
- parametric mask layout and verification

You will design a small chip that will be actually fabricated and characterized

Ghent University

- 19-23 June
- 4-5 September
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