An Optical Parallel Adder Towards Light Speed Data Processing

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History of Optical Computing

**Opt. computers**

Intensively studied in 1970’s, but CMOS computers are much more superior to the optical computers.

- Based on optical filters
  - Shadowgram
  - Tanida, Ichioka, JOSA 73, 800 (1983)
  - Hard to miniaturize

- Based on optical transistors
  - SEED (Bell Labs.)
  - Miller et al., OQE 22, S61 (1990)
  - Lower performance than CMOS

**Opt. interconnect**

In 2000’s, optical interconnects got into computers.

- Intel, IBM, PETRA lead investigation (Si photonics)
- Electronics → computation
- Optics → communication
- Only for interconnect?

- System in Package
- CPU, Optical interconnect
Beyond Optical Communication

- Chip-to-chip interconnect
  - DRAM
  - CPU/GPU

- Intra-rack optical interconnect

- Inter-rack optical interconnect

- Network-on-Chip
  - Optical accelerator
  - Optical accelerator
  - Optical accelerator
  - Optical accelerator
  - Optical accelerator

Our focus in this talk

- Optical Interface
  - Functional Unit

- RAM
  - Functional Unit

- CMOS CPU
  - Optical accelerator
  - Optical accelerator
Photonic Crystal Optical Pass Gate

Electrical Voltage Control
1: pass / 0: cross

Targeting 100 µm or less

~ 1 ps

Directional Coupler

Optical signal

Photo Detector

Electrical Voltage
1: pass / 0: block

< 1 ps

1.55 µm light

InAlAs

L = 1.7 µm

p-InP

n-InP

8 µm

Electrical Voltage
1: block / 0: pass

n-InP

L = 1.3 µm

C = 0.6 fF
Why Optical PG for Data Path?

- Good at data path operation
  - Light speed operation
    - Good at serial connection (light speed)
    - NOT good at cascade connection (OE & switching delay involved)
  - Good at pass/cross propagations (XOR and MUX)
Optical Parallel Adder Example

• Computation can be done by just passing the optical signal through the “pass gates”
Arithmetic Operation with OPG

- XOR/MUX-dominant data-path operation
  - Parallel Adder, Multiplier, and Barrel Shifter etc.

- Parallel adder as a first step
  - Can be constructed with serial connections only
Optical Full Adder

Library Cells in OptiSPICE simulator (Opto-electronic circuit simulator)

1: through
0: cross

Phase shifter
OE conversion
Y splitter
X coupler

Full Adder (AOI logic)

Full Adder (OPG logic)

All optical XOR

XOR
Design and Evaluation: 16-bit Adder

1: through
0: cross

Phase shifter
OE conversion
Y splitter
X coupler

π

 OE

X ⊕ Y (O)

X ⊕ Y (E)

Single Stage

Light propagation

X (O)

99

1

C_i+1

S_i

C_i

C_i+1

99

1

X ⊕ Y

X

Y

C_0

C_0

FA

C_1

C_1

FA

C_2

C_2

C_n-1

C_n-1

FA

X_0 Y_0

X_1 Y_1

X_{n-1} Y_{n-1}

S_0

S_1

S_{n-1}

OE conversion

π

OE

X (O)

X (O)

π

OE

OE conversion

π

OE

Design and Evaluation: 16-bit Adder

1: through
0: cross

Phase shifter
OE conversion
Y splitter
X coupler

π

 OE

X ⊕ Y (O)

X ⊕ Y (E)

Single Stage

Light propagation

X (O)

99

1

C_i+1

S_i

C_i

C_i+1

99

1

X ⊕ Y

X

Y

C_0

C_0

FA

C_1

C_1

FA

C_2

C_2

C_n-1

C_n-1

FA

X_0 Y_0

X_1 Y_1

X_{n-1} Y_{n-1}

S_0

S_1

S_{n-1}

OE conversion

π

OE

X (O)

X (O)

π

OE

OE conversion
OptiSPICE Simulation Results

- Optoelectronic Circuit Simulator (HSPICE engine)
- Light-speed parallel adder operation confirmed
  - Per digit delay: $\sim 1$ ps, Initial OE and switching delay: $\sim 25$ ps

![OptiSPICE Simulation Results Diagram]
16-bit CMOS Adder as Comparison

16 nm High Performance CMOS Technology PTM

Single digit carry propagation delay = 21.7 ps

Output Voltage [V]

Time [ps]
Comparison

• 16-bit parallel adder is designed with OPG
• Light-speed operation is confirmed
  – Per digit delay: OPG ~1 ps, CMOS 22 ps
  – 16-bit total delay: OPG ~40 ps, CMOS 350 ps
Wavelength Division Multiplexing

- Exploit WDM for reducing the circuit size
- \( \lambda_1 \) represents carry, \( \lambda_2 \) represents carry bar

Only \( \lambda_2 \) is given to the 1st digit carry input

Wavelength selective splitter
OptiSPICE Simulation Results

- Different wavelengths for carry and carry bar
  - This structure reduces RC delay in electric control signal
  - Per digit delay: ~1ps, Initial OE and switching delay: ~25ps

![Diagram showing output power vs time for different digits]

- LSB
- 1st digit Y
  - Input signal
- 1st digit X
  - Input signal
- 1st digit SUM
- 16th digit SUM
- Wave becomes steeper
- 20 ps
- 16th digit SUM
Related Work

- Parallel adder based on shared BDD


72% loss per digit
Max fan-out = 4
Large power loss
Serial connections = # digits x 2
Large power loss
Summary

• 16-bit parallel adder is designed with OPG

• Light-speed WDM operation confirmed
  – Per digit delay: OPG ~1 ps, CMOS 22 ps
  – 16-bit total delay: OPG ~40 ps, CMOS 350 ps

• Power loss is an issue to be resolved
  – Per digit power loss ~20%

• Future work
  – Extend this to more complicated functions
Acknowledgement

This work is partly supported by CREST (Core Research for Evolutional science and Technology) of JST (Japan Science and Technology Corporation)
Backup
Results of OptiSPICE Simulation

- Optoelectronic Circuit Simulator (HSPICE engine)
- Light-speed parallel adder operation confirmed
  - Per digit delay: \(~1\text{ps}\), Initial OE and switching delay: \(~10\text{ps}\)
  - 8-bit CMOS adder with 16nm HP PTM: 174 ps

![Diagram showing normalized power over time with carry and digit markers.]
Power Loss in Adder Operation

Power halves every 2 digits

1% loss in carry

Power splitter loss

99% loss in sum

Pass gate insertion loss

1db loss

- Power splitter loss
- 1% loss in carry
- 99% loss in sum
- Pass gate insertion loss
- 1db loss

- Power halves every 2 digits

- X\oplus Y \ (O)\quad X\oplus Y \ (E)

- OE

- C_i

- 99

- 1

- \pi

- X_0 \quad Y_0

- X_1 \quad Y_1

- X_{n-1} \quad Y_{n-1}

- C_0

- C_1

- C_2

- C_{n-1}

- S_0

- S_1

- S_{n-1}